A CMOS DB-LINEAR VGA WITH DC OFFSET CANCELLATION FOR DIRECT-CONVERSION RECEIVER

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Abstract

In this thesis, a CMOS dB-linear variable gain amplifier (VGA) with a novel I/Q tuning loop to remove DC offset for direct-conversion receiver has been designed in a 0.35μm CMOS technology.

The dB-linear VGA comprises a linear VGA and a novel pseudo-exponential voltage circuit. Different VGA and pseudo-exponential circuit have been studied. The proposed circuit is a differential source degenerated VGA and a Taylor's series expansion based pseudo-exponential voltage circuit, which has been designed, simulated, and tested.

Different DC offset cancellation methods have been investigated and a novel I/Q tuning loop is presented. DC offset sense issues have been discussed and solutions are presented. Block level simulation, circuit level simulation and measurement result are explained.

This dB-linear VGA provides a variable gain of 60dB while maintaining its 3 dB bandwidth greater than 2.5 MHz. DC offset rejection is 50 dB. The overall IIP3 and IIP2 is 12.165dBm and 40.7dBm, respectively.

Keywords: dB-linear, DC offset cancellation, I/Q mismatch, I/Q tuning loop, Pre-distortion compensation, VGA

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Contents

Summary

In this thesis, a CMOS dB-linear variable gain amplifier (VGA) with a novel DC offset cancellation scheme for direct-conversion receiver has been described.

The dB-linear VGA comprises a linear VGA and a newly proposed pseudo-exponential voltage circuit. Different VGA and pseudo-exponential circuit have been studied. From the requirement in DCRs, the proposed circuit is a differential source degenerated VGA and a Taylor's series expansion based pseudo-exponential voltage circuit, which has been designed, simulated, and tested.

Among all the mentioned inherited problems with direct conversion, DC offset may be the most severe problem. Therefore, DC offset cancellation is indispensable in zero-IF circuit of DCR. Different DC offset cancellation methods have been investigated and a novel I/Q tuning loop is presented. DC offset sense issues have been discussed and solutions are presented. System level simulation, circuit level simulation and measurement result are explained.

In summary, the CMOS dB-linear VGA provides a variable gain of 60dB while maintaining its 3 dB bandwidth larger than 2.5 MHz. non-ideal effects on

dB linearity are analyzed and the corresponding compensation methods are suggested. The proposed I/Q tuning loop is proved to be effective in removing DC offset and can suppress I/Q mismatch effects simultaneously. Measurement results based on 0.35-μm CMOS technology are presented to demonstrate the good linearity of the proposed dB-linear VGA and shows that the DC offset cancellation loop can remove DC offset efficiently.

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Symbols

a, b	Constants
A	Loop gain
A_v	Voltage Gain
$C_{I,\text{int}}$	Capacitance of integrator of I path
C_L	Load capacitance
C_{LPF}	Capacitance used for low pass filter
C_{ox}	Gate oxide capacitance per unit area
$C_{Q,\text{int}}$	Capacitance of integrator of Q path
e	Error voltage between DC offset and feedback tuning voltage
g_b	Equivalent transconductance of the V-I converter
g_m	Transconductance of the input transistor
G_s	Transconductance of the source degeneration
I_0	Bias current of the current square circuit
I_b	Bias current
I_{bias}	Bias current

I_{CS}	Constant current
I_{CM1}	Compensation current
I_{fI}	Feedback current of I path
I_{fQ}	Feedback current of Q path
I_{in}	Input current
I_{out}	Output current
I_{VI}	Output current of V-I convertor
k_{1I}	Amplifying weight for I path signal
k_{1Q}	Amplifying weight for I path signal
k_2	Amplifying weight for multiplied signal
k_b	Current mirror scale
k_{inte}	Amplifying coefficient of integrator
k_l	Amplifying coefficient of limiter
k_m	Amplifying coefficient of multiplier
L	Length of the transistor
M	Transistor
PI	Tuning direction of I path
PQ	Tuning direction of Q path
R	Resistor
R_{1I}	Equivalent output resistance of the low pass filter in I path
R_{1Q}	Equivalent output resistance of the low pass filter in Q path

R_d	Load resistor
R_e	Resistor to generate exponential voltage
R_I	Output resistance of the buffer of I path
R_L	Load resistance
R_{LPF}	Equivalent output resistance of the low pass filter
R_Q	Output resistance of the buffer of Q path
s	Laplacian
$sign(\cdot)$	Polarity
U	Product of DC offset of I path and Q path
V_0	Input of the varying bandwidth circuit
V_1	Signal amplitude after the low pass filter
V_{1I}	Output signal amplitude of I path low pass filter for polarity
V_{1Q}	Output signal amplitude of Q path low pass filter for polarity
V_c	DC voltage
V_{ctrl}	Gain control voltage
V'_{Ctrl}	Gain control voltage after pre-distortion compensation
V_{dc}	DC offset
V_{dcI}	DC offset of I path
V_{dcQ}	DC offset of Q path
vdd	Voltage supply

V_f	Feedback voltage
V_{high}	High voltage level of limiter
V_I	Total signal of I path
V_{low}	Low voltage level of limiter
V_m	Output of the multiplier
V_g	Gate voltage
V_{gs}	Gate-source voltage
V_{in}^c	Input voltage of the pseudo-exponential voltage circuit to generate gain control voltage
V_{in1}	The first input
V_{in2}	The second input
V_{inI}	Input signal of I path
V_{inQ}	Input signal of Q path
V_{inte}	Output of integrator
V_{out}	Output voltage
V_Q	Total signal of Q path
V_s	Source voltage
V_{st}	Sum of source voltage and threshold voltage
V_{sum}	Sum voltage signal
V_{th}	Threshold voltage
W	Width of the transistor
x	Independent variable

Y_{II}	Transconductance of the input transistor of the low pass filter for polarity deciecion in I path
Y_{IQ}	Transconductance of the input transistor of the low pass filter for polarity deciecion in I path
$Y_{I,\text{int}}$	Equivalent transconductance of the integrator of I path
$Y_{I\text{-}VI}$	Equivalent transconductance of the V-I converter of I path
Y_{LPF}	Transconductance of the input transistor of the low pass filter
$Y_{Q,\text{int}}$	Equivalent transconductance of the integrator of I path
$Y_{Q\text{-}VI}$	Equivalent transconductance of the V-I converter of IQ path
Z	Ac components of the output signal of multiplier
ω_{LPF}	Bandwidth of the low pass filter
μ_n	The mobility of electron
λ	Channel length modulation coefficient

Abbreviations

ADC	Analog-to-Digital Converter
AGC	Automatically Gain Control
BER	Bit error rate
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CDMA	Code division multiple access
CMFB	Common-mode feedback

CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common-mode rejection ratio
CSC	Current Square Circuit
DC	Direct Current
DCR	Direct Conversion Receiver
DSB	Double sideband
DSP	Digital Signal Processing
ESD	Electrostatic discharge
FSK	Frequency shift keying
GSM, GSM900	Global system for mobile communications
HPF	High Pass Filter
IC	Integrated Circuit
IF	Intermediate Frequency
IIP2	Second-order input intercept point
IIP3	Third-order input intercept point
IS-95	Interim standard 95
ISI	Inter-Symbol Interference
LNA	Low noise amplifier
LO	Local Oscillator
MOS	Metal oxide semiconductor
MOSFET	Metal oxide semiconductor field effect transistor
NF	noise figure

NMOS	N-channel metal oxide semiconductor
PCB	Printed circuit board
PGA	Programmable-gain amplifier
PMOS	P-channel metal oxide semiconductor
PTAT	Proportional to absolute temperature
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
SNR	Signal-to-noise ratio
SSB	Single sideband
SAW	Surface Acoustic Wave
TDMA	Time division multiple access
THD	Total harmonic distortion
VGA	Variable Gain Amplifier
WCDMA	Wide-band code division multiple access
WLAN	Wireless Local Area Network

Chapter 1

Introduction

1.1 Background and motivation

The evolution of current wireless communication systems has been very rapid. Complexity, cost, power dissipation, and the number of external components have been the primary criteria in selecting receiver architecture. While transistor technology scaling and improved circuit techniques will contribute evolutionary advances towards this goal, architectural innovations in the transceiver may lead to revolutionary improvements. It is in this context that there is a resurgence of interest in Direct-Conversion. Although superheterodyne used to be employed commonly in wireless communication receivers for a long time, direct frequency conversion has emerged over the last six years as the de-facto standard for GSM handset design. Among the handset manufacturers currently using direct conversion architectures are Alcatel, nokia, Ericsson, Samsung, Siemens to name a few. Also, several RFIC suppliers (Infineon, Conexant, Analog Devices, Phillips, Qualcomm, TI, etc.) are currently offering standard direct conversion chipsets for

GSM handsets and have started to offer the same for WCDMA and CDMA systems.

Variable Gain amplifier is an important block in the base-band circuit in the DCR architecture. A VGA is typically used in a feedback loop to realize the AGC circuit. The demand of an automatic gain control (AGC) loop in wireless system comes from the fact that all communication systems have an unpredictable received power. To buffer receiver electronics from change in input signal strength by producing a known output voltage magnitude, an AGC loop is indispensable in DCRs [1]. Therefore, with a VGA, dynamic range of the overall system is greatly improved. To maintain AGC loop settling time which is independent from the signal levels, an exponential gain control characteristic is required [1]. A VGA should meet requirements of large dynamic range and good dB linearity. And for DCR applications, it has to be able to efficiently suppress DC offset.

DC offset is a severe problem in DCRs. DC offset comes from device mismatch and local oscillator leakage. Since device mismatch and local oscillator leakage always exist, DC offset is an inherent problem of DCRs. Because in a direct-conversion receiver the down converted band extend to zero frequency, extraneous offset voltages can corrupt the signal and, more importantly, saturate the following stages [2]. Therefore, offset cancellation methods are necessary in DCRs. An extensive review of DC offset cancellation methods is given in 2.2, and the drawback of these methods is analyzed. Currently, DC offset cancellation is still a demanding task in DCRs and more research needs to be done.

In this thesis, a CMOS dB-linear variable gain amplifier (VGA) with a novel I/Q tuning loop for DC offset cancellation for direct-conversion receiver has been designed in a 0.35μm CMOS technology. With some minor modification, this proposed VGA can be used for different applications in wireless communication, such as WLAN, WCDMA.

1.2 Thesis organization

In Chapter 2, a comprehensive review of DCRs, VGAs, and DC offset cancellation solutions is given. Basic architecture of DCR is described and its advantages and challenges are studied. Previously reported methods of implementing dB-linear VGA and DC offset cancellation circuits have been investigated.

In Chapter 3, the system configuration of the proposed VGA circuit is described. Also, an introduction to the VGA circuit requirements is given. These requirements depend on the system specifications, receiver architecture, and receiver partitioning.

Chapter 4 concentrates on the design of the dB-linear VGA. First a linear VGA is described. Then a novel exponential voltage generator is proposed to obtain the dB-linear control characteristics. Next the non-ideal effects on dB linearity are analyzed and the corresponding compensation methods are suggested. At last simulation result is shown.

Chapter 5 describes a novel DC offset cancellation circuit for DCR. The proposed structure uses an I/Q tuning loop to remove DC offset. I/Q mismatch issue is discussed and the solution to suppress I/Q mismatch effects is adopted. A variable bandwidth technique is employed to accelerate the loop acquisition when the system is first time turned on. Moreover, a tuning scheme is adopted to efficiently suppress effects of I/Q mismatch. At last simulation results based on block level and circuit level is shown.

Chapter 6 describes the experimental result to demonstrate the effectiveness of the pre-distortion techniques and the DC offset tuning loop.

Chapter 2

Literature Review

2.1 Direct-conversion receivers

Increased pressure for small form factor, low cost, reduced bill of materials and low power consumption in radio application have triggered the industry to resurrect the direct conversion transceiver radio architecture. Although direct-conversion receiver approaches have been studied for decades, only recently when the high-performance components are available, the direct-conversion architecture becomes practical for a wide range of wireless applications.

2.1.1 Architecture of Direct-conversion receivers

The direct-conversion receiver (DCR) architecture, as shown in Fig.2.1, can achieve similar performance to the superheterodyne ones, but with less complexity. In DCR, the received signals are amplified with a fixed-gain LNA after the first RF preselection filter. Subsequently, the RF signals are directly downconverted to

in-phase (I) and quadrature (Q) baseband signals without an intervening IF stage. After the RF signals are demodulated to the baseband, individual channel selection is performed using a baseband channel-select filter. The baseband filter is more compact and less expensive than the superheterodyne receiver's IF channel-select filter. In addition, the baseband channel-select filter can be designed with variable bandwidth, facilitating multi-mode or multi-standard operations.

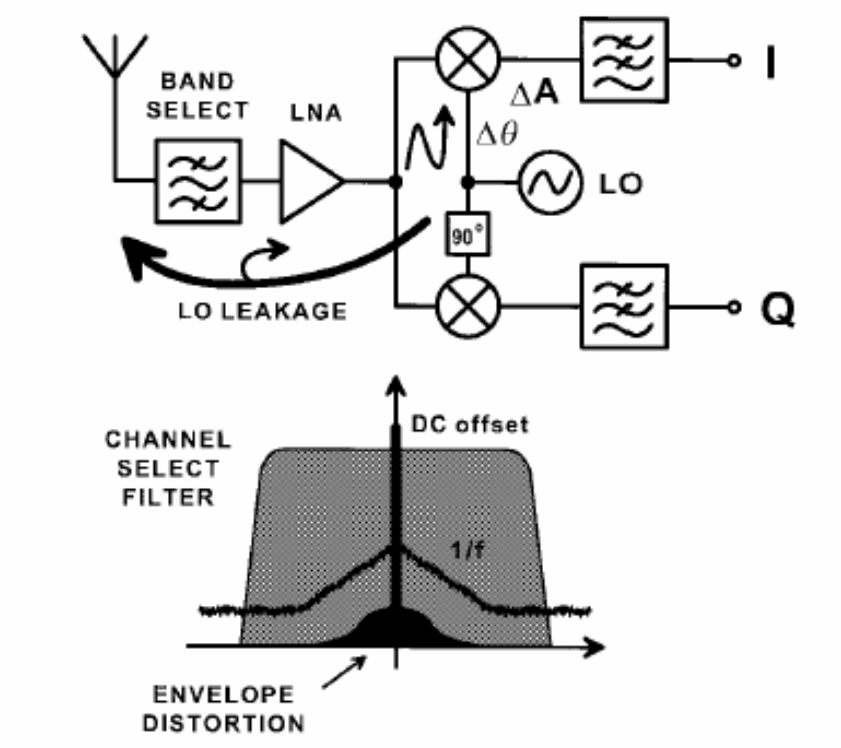


Fig.2.1 Direct-conversion Principle and downconverted spectrum

Although baseband channel-select filters offer a great deal of flexibility, the composite baseband signals contain all of the adjacent-channel blocking signals that are normally filtered before they reach the I/Q demodulator (see Fig.2.1). As a result, the direct-conversion-receiver's I/Q demodulator must provide a dynamic

range as wide as 80 dB.

2.1.2 Merits and design issues of DCRs

Direct conversion has several advantages over super-heterodyne receivers. A DCR simplifies the frequency planning and eliminates the IF surface acoustic wave (SAW) filter required in super-heterodyne receivers. As a result, only a single local oscillator (LO) signal is required, and the image issue is also eliminated. Thus, the part count in DCR is reduced, leading to lower cost and smaller size. Additionally, higher levels of RFIC integration is possible. This becomes increasingly important as the complexity of the handset radio is loaded with the additional features, such as GPS, Bluetooth, WLAN, and multistandard support (such as various combinations of CDMA, WCDMA, GSM, and so forth) [3].

However, direct translation of the spectrum to zero IF frequency also entails a number of issues that do not exist or are not as serious in a heterodyne receiver. The main issues that need to be dealt with in DCR design are DC offset, I/Q Mismatch, Even-order Distortion, Flicker noise and LO-leakage. Among them, the DC offset is the most severe problem.

2.2 dB-linear VGA

Variable Gain Amplifier (VGA) is very important in wireless communication systems. This is because all wireless communication systems have an

unpredictable received power and an automatic gain control (AGC) loop is needed. A VGA is typically used in a feedback loop to realize the AGC circuit to buffer receiver electronics from the change in input signal strength by producing a known output voltage magnitude [4]. In an AGC loop, an exponential gain control characteristic, or called dB linearity, may be required to maintain the settling time independent of the input signal levels and achieve a large dynamic control range [5].

A lot of work has been done on dB-linear VGA. Generally, there are tow types of dB-linear VGA. One is a VGA who has the inherent dB-linear gain characteristic. The other is a linear VGA whose gain is controlled by an exponential voltage or current.

Many inherent dB-linear VGAs are implemented based on bipolar technology because of its exponential characteristic between the current and voltage. In CMOS technology, the implementation is not straightforward because of its square-law characteristic in strong inversion. Several inherent dB-linear VGAs realized in CMOS have been reported[6, 7, 8, 9, 10, 11, 12, 13]. These circuits compose a special structure to make the current or voltage relationship approximate the exponential characteristic. Therefore, it is difficult to achieve small approximation error and the large dynamic range of the gain.

A dB-linear VGA can also be implemented by a linear VGA with an exponential gain control characteristic. Because of the needs for wide dynamic range, precise gain control, low noise figure and good linearity, the design of such

a VGA is a demanding task.

2.2.1 Linear VGA

There are two possible ways to build a VGA. One is a fixed gain amplifier follows a programmable attenuator, the other is the cascade of variable transconductors.

In [10, 14, 15], VGA circuits implemented by the first method are reported. This approach has the advantage that the amplifier may be optimized for high gain and low noise figure, and the attenuator yields an arbitrarily wide range simply by adding more stages to the ladder. However, this method has its drawbacks. Firstly, it enforces a fundamental relationship between overall gain, noise figure, and output distortion. Over most of the gain range, the VGA noise figure tracks the attenuator loss. Secondly, as the attenuator is assumed perfectly linear, the fixed amplifier determines intermodulation distortion. Therefore, whatever the VGA gain setting, the amplifier input is always at the same level, and the output IM3 is constant. Both these properties are unfavorable [16]. Thirdly, if an amplifier is composed of a variable attenuator and a small-signal amplifier block, the insertion loss of the attenuator in front of the amplifier block directly degrades the noise figure of the amplifier. This results in a reduction of dynamic range because of the increase of the noise at the low signal-level end [17].

A second way to build VGA is with a cascade of variable transconductors. VGA circuits implemented by this method can overcome problems discussed

above. In CMOS technology, basically there are four methods to control the gain of a VGA, namely, (1) by varying the tranconductance of a MOS device operated in the saturation region, (2) by varying the load resistance, (3) by varying the source degeneration resistance which is often implemented by a MOS device operated in the linear region and (4) a multiplier-like topology.

The first method entails varying the bias current of the MOS device [11, 18, 19]. Since the transconductance of a MOS device varies as the squared root of the bias current, the bias current has to be varied as a square function of the gain variability desired. This entails a lot of power dissipation to obtain gain variation [20].

The gain of the VGA can also changed by adjusting load [21, 22]. Since the load normally determines the dynamic range of the amplifier, this method can not provide large gain variable range. Continuous control in gain variation is also difficult to achieve.

Gilbert cell is widely used in multiplier-like topology to realize a VGA [23, 24, 25]. Although g_m of a single short-channel MOSFET depends only weakly on current, the net transconductance of a Gilbert topology may be swept from zero to a maximum value. Thus it is well suited to provide large gain to small input signals, and it may be designed for low noise.

Variable source degeneration is also commonly used for varying the gain of the VGA. This does not have the drawbacks of varying bias current or load resistance. Since the source degeneration does not consume any additional current, no change in the bias current is necessary to achieve the gain variation[20]. Besides the low power dissipation, a differential pair degenerated by a MOSFET resistor has the advantage of good linearity.

2.2.2 Pseudo-exponential circuit

In order to implement dB-linear characteristic, a pseudo-exponential voltage circuit is needed to control the gain of the linear VGA. It is a simple way to use digital signal processor (DSP) to generate exponential voltage. High dynamic range and small error can be expected [26, 27]. However, the use of a DSP implies that the generated exponential is not continuous [28]. In most applications, continuous exponential voltage is needed. Thus, it gains attention to generat exponential by analog methods.

Traditionally, the exponential input circuit is implemented in bipolar technology due to the exponential characteristics [29]. However, bipolar technology are not compatible for monolithic CMOS-based analog and mixed-signal circuits. On the other hand, BiCMOS technology may not be cost effective [30].

Although MOS transistors in weak inversion exhibit exponential I-V characteristics [31, 32], their performance is poor in terms of speed and bandwidth

[30]. Thus it is only limited to low frequency applications. In strong inversion, due to its inherent square-law or linear characteristics, some approximation has to be employed to realize exponential voltage or current in CMOS.

Generally, two methods are widely employed to approximate an exponential function. One is a pseudo-exponential function, that is,

$$e^x \approx \left(\frac{1+x}{1-x}\right)^n \tag{2.1}$$

An implementation based on (2.1) with $n=\frac{1}{2}$ was reported in [33]. The approximation approach used in this implementation has two drawbacks. Since the current control of transconductance is used, the gain is limited by the square-root nature of the device to a fairly small range. Also, the signal path linearity is not very good unless large V_{gs} voltage are used. Other implementations based on the approximation in (2.1) with n=1 were reported in [34, 35, 36]. The approximation error is within 5% when $|x| < 0.32$. The approximation errors of this pseudo-exponential function to the ideal one will be reduced as n goes up. With n=2, equation (2.1) holds valid for $-0.24 < x \le 0.24$ with a 2% error [37, 38, 39]. Typically, the "pseudo-exponential" approximation is of particular interest since it provides large dB-linear range (about 15 dB with the error $< \pm$ 0.5dB. However, it is difficult to implement due to the requirement of the division function, i.e., (1+x)/(1-x) [30].

Taylor's series given in (2.2) is an alternative method to approximate the exponential function [31, 40, 41, 42],

$$e^{ax} \approx 1+\frac{a}{1!}x+\frac{a^2}{2!}x^2+\frac{a^3}{3!}x^3+\cdots+\frac{a^n}{n!}x^n \tag{2.2}$$

Since MOS transistors have square law characteristic in saturation region, the Taylor approximation, which follows a squaring function and comprises only additive functions, is easily implemented [16].

Mathematically, the exponential function can be approached with small deviation by high order Taylor's series. The major deviation of exponential function results from the ignored high-order terms in the Taylor's series, the absolute range of x and the coefficient "a". Obviously, if $a \geq 1$ and $x \geq 1$, exponential function can not be implemented by only the low-order polynomial. It can be shown that the truncation error of the Taylor's series can be less than 5% if $-0.575 \leq x \leq 0.815$ is satisfied [43]. Obviously, Taylor's series approximation has a larger input dynamic range than the pseudo-exponential method for the same approximation error.

A CMOS exponential current-to-voltage circuit based on another approximation method was reported in [44]. The approximation is given as

$$e^{ax} = \frac{e^{ax/2}}{e^{-ax/2}} \cong \left[\frac{k+\left(1+ax/2\right)^2}{k+\left(1-ax/2\right)^2}\right]. \tag{2.3}$$

For k = 1, the numerator and denominator in (2.3) are same as the Taylor's series approximation. However, for the k slightly less than unity, the dB-linear range of (2.3) is extended drastically.

Some other approximation methods given in (2.4) to (2.6) was reportee in [35],

$$\exp(x)=\frac{\exp(ax)}{\exp\left(-(1-a)x\right)}\approx\frac{1+ax}{1-(1-a)x} \tag{2.4}$$

$$\exp(x)=\frac{\exp\left(\frac{x}{2}\right)}{\exp\left(-\frac{x}{2}\right)}\approx\frac{1+\frac{x}{2}}{1-\frac{x}{2}} \tag{2.5}$$

$$\exp(x)=\frac{\exp\left(\frac{3x}{4}\right)}{\exp\left(-\frac{x}{4}\right)}\approx\frac{1+\frac{3x}{4}}{1-\frac{x}{4}} \tag{2.6}$$

(2.4)-(2.6) are not widely employed in the implementation of exponential function because special circuit structure is needed to make the coefficients match the equation.

2.3 DC offset cancellation

2.3.1 Degeneration and impact of DC offset

It will be helpful to understand the origin and the impact of the offsets. The dc offset from a mixer consists of a constant and time-varying components.

The constant DC-offset can be attributed to the mismatch between the mixer components in the analog circuit. This type of DC offset is inherent to the circuit

and does not vary with time. Good design and layout can reduce the leakage and imbalances that cause this DC-offset [47].

Time-varying DC-offset is more harmful, it is generated by self-mixing, includes self-mixing of LO and self-mixing of the RF signal.

First, self-mixing of LO is caused by local oscillator leakage back into the antenna port of the terminal or by circuit imbalances [48]. Because this type of DC-offset only varies slowly, it is often considered fixed over the packet duration. However, the problem of this type of DC-offset may be exacerbated if the DC-offset is time-varying. This occurs when the LO signal leaks to the antenna and is radiated and subsequently reflected from moving objects back to the receiver. For example, when a car moves at a high speed, the reflections may change rapidly.

Second, self-mixing of RF signal is caused by signal leakage from the radio frequency (RF) input to the local oscillator port or by circuit imbalance combined with nonlinearity within the mixer. This is illustrated in Fig. 2.2. The isolation between the LO port and the inputs of the mixer and the LNA is not perfect, i.e., a finite amount of feedthrough exists from LNA or mixer input to LO port. This effect arises from capacitive and substrate coupling. If the LO signal is provided externally, this could happen through bond wire coupling. The leakage signal appearing at the inputs of the mixer is now mixed with itself, thus producing a dc component at point C. This phenomenon is called “self-mixing.” The input RF signal to mix with itself creates a distortion signal whose amplitude is proportional

to the RF input signal's power envelope [9].

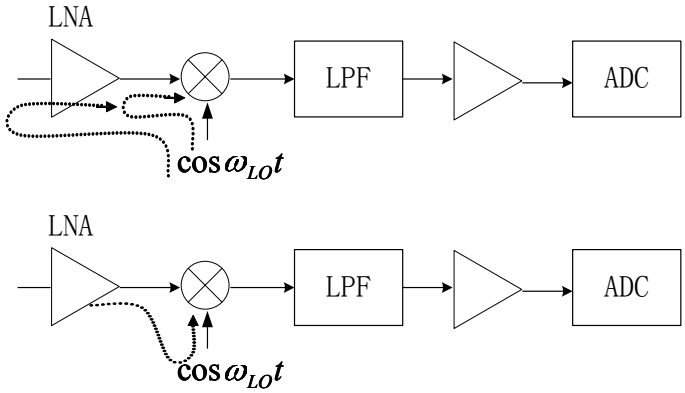


Fig.2.2 Mechanism of DC offset generation

Performance of the receiver can be severely degraded by DC-offset. First, the DC-offset may appear at the center of the desired signal down-converted to the baseband stage and distort the signal [46]. The DC-offset may dominate the signal strength by as much as 50 -100 times in amplitude and substantially degrades the bit error probability [50]. Moreover, in direct conversion receivers, the mixer is immediately followed by a chain of high-gain directly coupled amplifiers that further amplify the dc offset and saturate the following stages. Consequently, sensitivity of the receiver can be directly limited by the dc-offset component of the mixer output [48]. Therefore, the offset must be removed in analog domain before sampling. Otherwise, it will saturate the baseband amplifiers, and results in a potentially devastating nonlinear signal distortion [50].

2.3.2 DC cancellation review

Several techniques have been proposed to suppress DC offset. These include 1)

AC coupling, 2) Digital signal processing (DSP), 3) DC offset subtraction, 4) Auto-zero, 5) even harmonic mixing, and 6) use of feedback configuration.

The AC coupling uses the coupling capacitor to block the DC offset[51, 52]. Fig.2.3 shows an example of capacitor isolation. It is an easy way to remove DC offset. However, this method requires large capacitor values that are not realizable on-chip [53]. Another drawback of AC coupling is that it can not be used for more spectrally efficient modulation schemes such as QAM, where the baseband signal spectrum has significant energy at low frequency [54]. In addition, AC coupling using large capacitor values often results in a failure to track fast variations in the offset voltage.

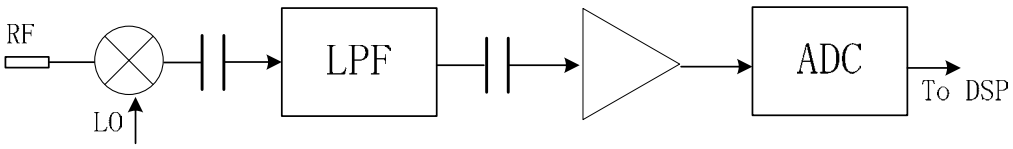


Fig.2.3 AC coupling for DC-cancellation

The second common approach to remove the DC offsets is to use DSP, where a digital cancellation algorithm is employed on the sampled signal before the decision device[55, 56]. In this approach the offset is detected and removed digitally by time-averaging or by using more complex methods such as differentiating the received signal. However, digital cancellation requires the analog baseband stages following the mixer to have sufficient spurious-free dynamic range (SFDR) in order to accommodate the large DC offset. It also requires analog-to-digital converter that consume a considerable amount of power.

In the DC offset subtraction approach, the offset is temporarily stored and

subsequently subtracted from the baseband path [57]. This is illustrated in Fig.2.4. It requires the ADC to have a larger dynamic range and an additional DAC.

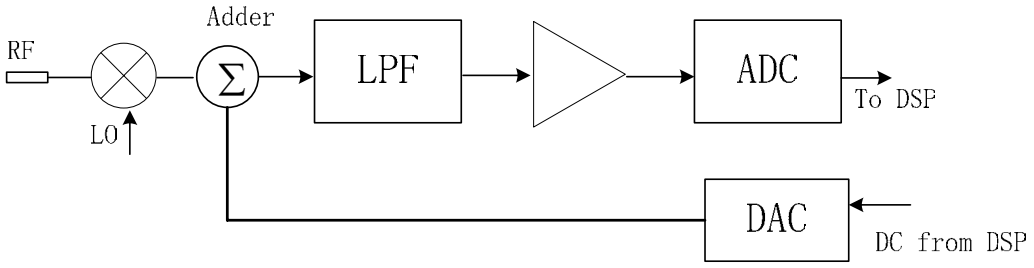


Fig.2.4 Feedback DAC system

The Auto-zero technique uses idle time between data bursts to measure the unloaded receiver intrinsic DC offset [58, 59]. In time-division multiple access (TDMA), each mobile periodically enters an idle mode so as to allow other users to communicate with the base station. This idle time can be used to measure the offset and subtract the value during the reception of the next burst. This approach only works if the offset can be assumed constant during the reception of at least two bursts (the burst used to measure plus the consecutive reception burst). For GSM, the time-variance of the offset due to fading is up to around 200Hz and can therefore be neglected due to the short burst time of 577ps. But there could be a potential problem for two unsynchronized TDMA. If the burst of an alien system stars during the reception, this could cause an abrupt change in DC offset due to interferer self-mixing. Therefore measuring the offset during idle time may not be accurate [57].

Another way to avoid low frequency noise being appended to the baseband signal is the use of the sub-harmonic mixers to increase isolation between RF and

LO signal [60, 61]. By choosing an even-order sub-harmonic mixer topology, an out-of-band LO can be used in place of the in-band counterpart to alleviate LO radiation and, consequently, reduce the time-varying component of the dc offset. Even-harmonic (EH) mixing using an antiparallel diode pair (APDP) has been introduced in previous works as a good candidate for such mixer topology [52, 62].

The last method of DC cancellation is to use the dc-coupled stage with a feedback configuration as depicted in Fig.2.6(a), [63, 64]. The dc extractor block proportionally converts the output offset voltage into the respective offset current fed into the MOS capacitor through a g_m block. The parallel resistor represents the finite output resistance in the g_m block. The integrated error voltage is subtracted from the input signal in the summer, which is embodied with an additional input pair in the PGA. The frequency response of dc-offset cancellation scheme is shown in Fig.2.6(b). This scheme is effective in that it does not incur any in-band loss and it is able to use the MOS capacitor which is several times smaller area than the floating counterpart. Varying the values of the resistor or MOS capacitor can easily alter the corner frequency of the high pass filter characteristics, and affect SNR performance and settling time.

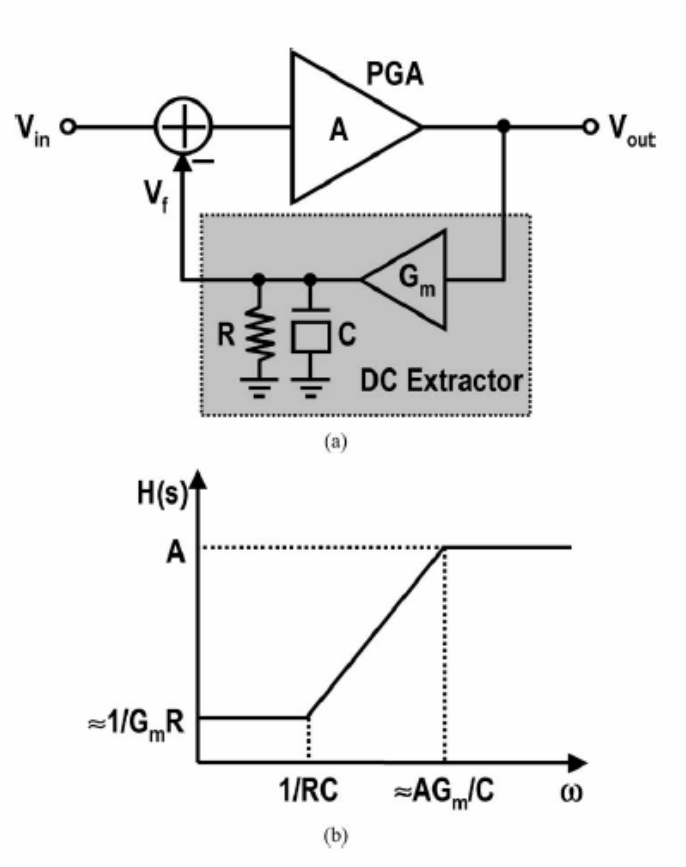


Fig.2.5 Feedback configuration to cancel DC offset. (a) Conceptual diagram. (b) Frequency response

Chapter 3

Receiver System Configuration

The architecture of the direct-conversion receiver is depicted in Fig.3.1. The input signal from the antenna is amplified by a LNA; then the desired signal is directly translated to the base-band by a mixer and is further amplified by VGA; the low-pass filter is employed to suppress nearby interferers. Analog-to-digital (A/D) converter is used to allow digital signal processing (DSP) circuits to perform demodulation and other ancillary functions. I and Q branches are employed because for most phase and frequency modulation schemes DCR must incorporate quadrature downconversion [65].

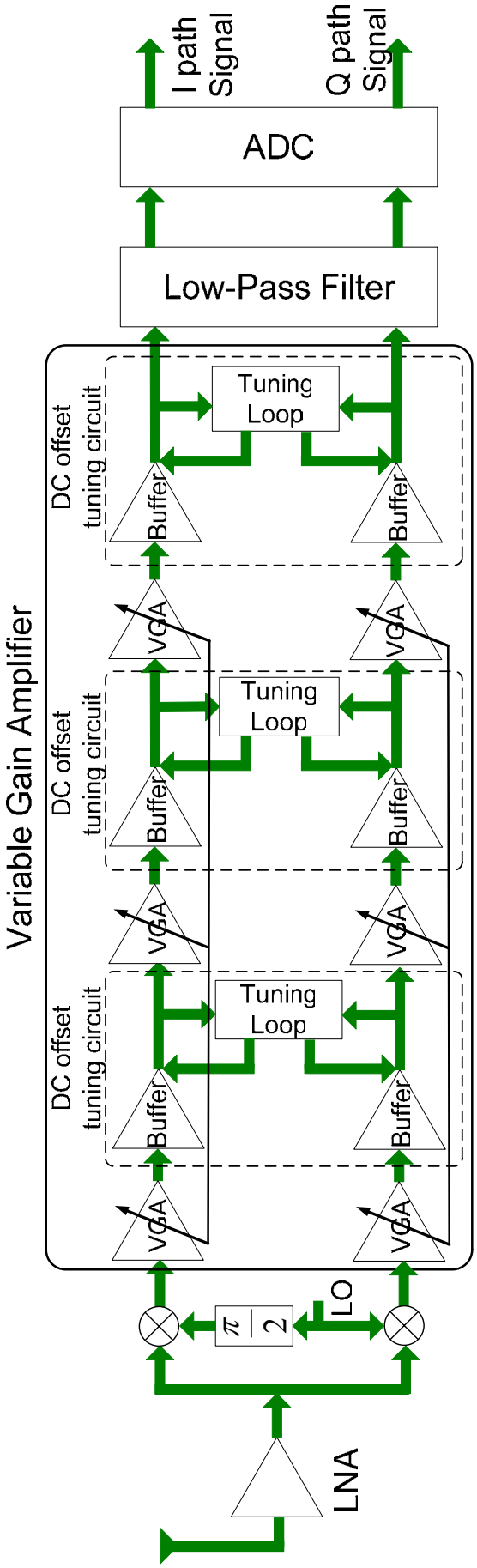


Fig.3.1 System Diagram

For WCDMA applications, receiver sensitivity is typically around –80 dBm and signal bandwidth is 5 MHz (double sided). As a result, the microvolt input signal from the antenna needs to be amplified around 100 dB to a level that can be digitized by a low cost, low power ADC. Of this gain, typically 25 to 30 dB is contributed by the LNA/mixer combination, and LPF may provide a gain of about 10 dB. Thus the VGA may need to provide the remaining gain of 60 dB. On the other side, the typical value of the DC offset appearing at the output of the mixer is on the order of 10 mV [65]. Thus, if it is directly amplified by such a high gain as 60dB provided by the VGA, the offset voltage will saturate the following circuits, thereby prohibiting the amplification of the desired signal [65]. To avoid the DC offset corrupting the demodulation of the desired signal, it is desirable to restrict DC offset at the output of VGA to less than several millivolts.

The architecture of the proposed VGA circuit is embedded in Fig.3.1. In each branch, three stages of proposed VGA are cascaded to provide 60 dB variable gain. A buffer is employed after each VGA stage. The buffer provides 0 dB gain, namely, it is not employed for signal amplifying but is involved in the DC offset tuning loop. Thus, signal amplifying and DC offset cancellation are separated. In each stage, one tuning loop is used in common by I and Q branches. The tuning loop uses feedback structure for DC offset detection and forming of tuning current, while employs feedforward canceling of DC offset. By this tuning scheme, quick tracking can be achieved.

The highest and lowest signal level from the mixer is -63dBV and -3dBV

espectively. To ensure that the output signal can drive the following ADC, the output level of VGA should be -3 dBV. Other specifications for the VGA proposed in this paper are listed in Table 1. With some minor modification, the proposed VGA can be used for several applications in wireless communications, such as Wireless LAN, WCDMA etc.

This thesis focuses on the VGA circuit. A CMOS dB-linear VGA which meets these specifications is illustrated. A novel exponential circuit is proposed to obtain the dB-linear control characteristics. The non-ideal effects on dB linearity are analyzed and the corresponding compensation methods are suggested to obtain good dB linearity.

Table 1 Specifications of proposed VGA

Input Level (dBV)		Output Level (dBV)	
High Gain Mode	Low Gain Mode	High Gain Mode	Low Gain Mode
-63	-3	-3	-3
Other Figures			
noise Figure (dB)	IIP3 (dBm)	IIP2 (dBm)	-3 dB Bandwidth (MHz)
10	10	40	2.5
Output DC offset			
< 10mV			

Chapter 4

A novel CMOS dB-Linear VGA

4.1 Differential linear variable gain amplifier

The proposed VGA is implemented using source-degeneration method to realize variable gain. Three identical VGA stages are cascaded to provide an overall gain of 60 dB. A pseudo-exponential voltage circuit is used to simultaneously control the gain of three VGA stages.

A single stage of the differential linear VGA is shown in Fig.4.1. M_3 and M_4 form the linear transconductance pair. M_5 and M_6 act as the active load to provide high gain. M_7 and M_8 are used to improve the linearity [66]. The common-mode feedback circuit consists of R_1, R_2 and M_{10}-M_{13}. The gain of the VGA can be adjusted continuously over a large range (~20dB) through the source degeneration transistor M_{14}. The gain of the VGA can be expressed as:

$$A_v = -G_s R_d \frac{g_m}{g_m + G_s} \tag{4.1}$$

where g_m, G_s and R_d represent the transconductance of the input transistor, the conductance of source degeneration transistor, and the load resistance, respectively. The conductance of the source degeneration transistor can be expressed as:

$$G_s = \mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_{gs} - V_{th}\right) \tag{4.2}$$

Obviously, if $g_m >> G_s$ and $g_m/\left(g_m + G_s\right) \approx 1$, A_v can be rewritten as

$$\begin{aligned} A_v &= -G_s R_d \frac{g_m}{g_m + G_s} \\ &\approx -\mu_n C_{ox}\left(\frac{W}{L}\right)_{14}\left(V_{gs14} - V_{th}\right) R_d . \end{aligned} \tag{4.3}$$

Therefore, A_v is a linear function of V_{gs14}, and the gain of the VGA can be linearly controlled by the gate voltage of M_{14}.

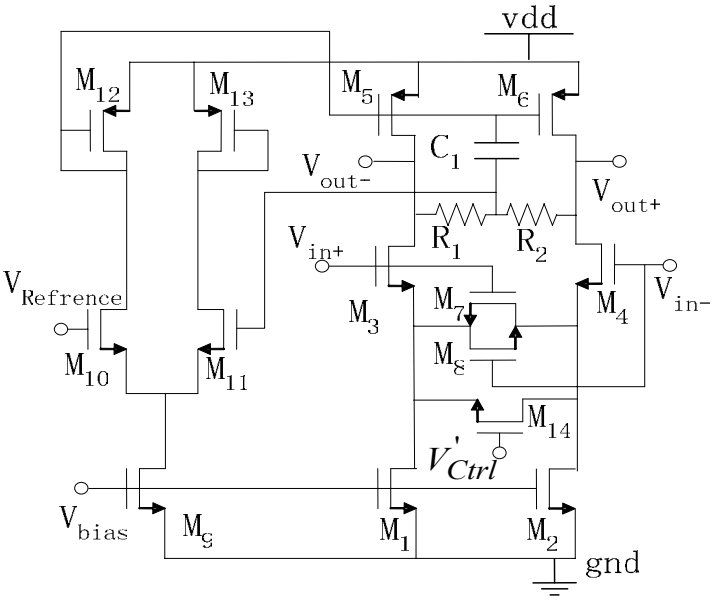


Fig.4.1 One stage of the differential linear VGA

4.2 Exponential function generation circuit

The Taylor's series expansion of a general exponential function can be expressed as

$$e^{\frac{b}{a}x} = 1 + \frac{b}{a}x + \frac{1}{2!}\left(\frac{b}{a}x\right)^2 + \frac{1}{3!}\left(\frac{b}{a}x\right)^3 + \cdots \frac{1}{n!}\left(\frac{b}{a}x\right)^n + \cdots . \tag{4.4}$$

where a and b are two constants. If $|bx/a| << 1$, the higher order terms are negligible, and (4.4) becomes

$$e^{\frac{b}{a}x} \approx 1 + \frac{b}{a}x + \frac{1}{2}\left(\frac{b}{a}x\right)^2 \tag{4.5}$$

Multiplying $2a^2$ at both sides of (4.5), we can arrive at

$$2a^2 e^{\frac{b}{a}x} \approx a^2 + (a + bx)^2 \tag{4.6}$$

From the analysis of Taylor's series approximation to exponential function in Chapter 2, a large range of x in (4.6) can be attained if the constant a and b are carefully chosen to ensure $-0.575 < bx/a < 0.815$. Changing circuit coefficients, such as transistor size or transconductance, can easily change *a* and *b*. Thus large dynamic range of *x* can be achieved. The approximation error is less than 5% if $-0.575 < bx/a < 0.815$ is met. Based on (4.6), a wide-range exponential voltage generation circuit is proposed and shown in Fig.4.2. It includes three building blocks, namely, a linear V-I converter [67], a constant

current source and a current square circuit (CSC) [68].

The output current of the CSC can be written as [68]:

$$I_{out} = 2I_0 + \frac{I_{in}^2}{8I_0} \tag{4.7}$$

The output current of the V-I converter can be expressed by $I_{VI} = 2g_b V_{in}^c$, where g_b is the equivalent transconductance of the V-I converter. By adding a constant current $I_{CS} = 4I_0$ to I_{VI} and assuming that the input current of CSC, $I_{in} = I_{VI} + I_{CS}$, as shown in Fig.4.2, the output current of CSC can be rewritten as

$$\begin{aligned} I_{out} &= 2I_0 + \frac{\left(I_{VI} + I_{CS}\right)^2}{8I_0} \\ &= \frac{1}{8I_0}\left[\left(4I_0\right)^2 + \left(4I_0 + 2g_b V_{in}^c\right)^2\right] \end{aligned} \tag{4.8}$$

By properly sizing the transistors, $-0.575 < 2g_b V_{in}^c / 4I_0 < 0.815$ can be ensured for the entire operation range of V_{in}^c. Using this condition and (4.6), (4.8) can be rewritten as:

$$\begin{aligned} I_{out} &\approx \frac{1}{8I_0} 2\left(4I_0\right)^2 \exp\left(\frac{2g_b}{4I_0} V_{in}^c\right) \\ &= 4I_0 \exp\left(\frac{g_b}{2I_0} V_{in}^c\right). \end{aligned} \tag{4.9}$$

Thus an approximately exponential current is realized. Furthermore, the exponential control voltage V_{ctrl} can be easily generated by passing the CSC output current through a resistor R_e, i.e.,

$$V_{ctrl} = R_e I_{out} = 4R_e I_0 \exp\left(\frac{g_b}{2I_0} V_{in}^c\right) \tag{4.10}$$

This voltage is used to control the gain of the linear VGA in Fig.4.1 and hence a dB-linear VGA is realized.

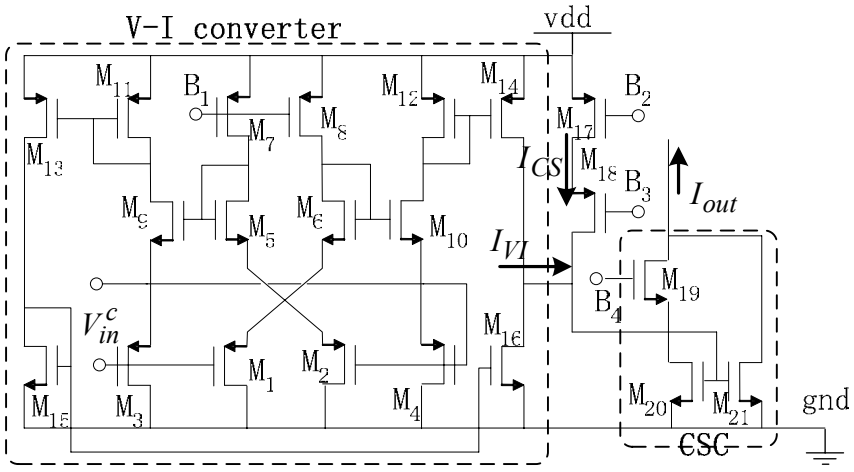


Fig.4.2 Pseudo-exponential voltage circuit

4.3 dB linearity compensation

Ideally, a linear VGA whose gain is controlled by an exponential function voltage would exhibit good dB linearity. However, in practice, it is affected by two factors: (i) the nonzero source voltage and the threshold voltage of the degeneration transistor M_{14} and (ii) the increase of G_s with V_{in}^c.

4.3.1 Compensation for nonzero source voltage and the threshold voltage of the degeneration transistor

Firstly, considering the effect of gate-source voltage and the threshold voltage of M_{14}, and since the gate voltage of M_{14} comes from the control voltage V_{ctrl}, (4.3) can be rewritten as:

$$\begin{aligned} A_v &= -\mu_n C_{ox}\left(\frac{W}{L}\right)\left(V_g - V_s - V_{th}\right)R_d \\ &= -K\left(V_{ctrl} - V_{st}\right)R_d . \end{aligned} \tag{4.11}$$

where $V_{st} = V_s + V_{th}$ and $K = \mu_n C_{ox}\left(W/L\right)$. Substituting V_{ctrl} into (4.11), A_v can be written as:

$$A_v = -KR_d\left[4R_e I_0 \exp\left(\frac{g_b}{2I_0}V_{in}^c\right) - V_{st}\right]. \tag{4.12}$$

Taking logarithm of both sides, it yields

$$20\log\left|A_v\right| = 20\log KR_d + 20\log\left[4R_e I_0 \exp\left(\frac{g_b V_{in}^c}{2I_0}\right) - V_{st}\right]. \tag{4.13}$$

Obviously, since V_{st} is not zero, the gain of the VGA will not be dB-linearly proportional to V_{in}^c. In a certain technology, V_{st} can be roughly estimated and for the nonlinearity compensation. To compensate the nonlinearity caused by the gate-source voltage and the threshold voltage of M_{14}, a fixed current $I_{CM1} = V_{st}/R_e$ is added to I_{out} and the control voltage becomes

$$V_{Ctrl}^{'} = \left(I_{out} + I_{CM1}\right) R_e = V_{Ctrl} + V_{st} \,. \tag{4.14}$$

Substituting it into (4.13) and taking logarithm of both sides, yields:

$$\begin{aligned} 20\log\left|A_v\right| &= 20\log KR_d + 20\log\left[4R_e I_0 \exp\left(\frac{g_b V_{in}^c}{2I_0}\right)\right] \\ &= 20\log\left(4KR_e R_d I_0\right) + \frac{10 g_b}{I_0} V_{in}^c. \end{aligned} \tag{4.15}$$

The effect of V_{st} is removed.

4.3.2 Compensation for the increased transconductance

Secondly, the gain linearity of the VGA is also affected by the dependence of G_s on V_{in}^c. To elaborate this, assuming the nonlinearity caused by V_{st} has been removed, substituting (4.10) into (4.2), G_s can written as

$$G_s = 4KR_eI_0 \exp\left(\frac{g_b}{2I_0}V_{in}^c\right). \tag{4.16}$$

With (4.16), the gain of the VGA can be expressed as:

$$A_v = -R_d g_m \frac{4KR_eI_0 \exp\left(\frac{g_bV_{in}^c}{2I_0}\right)}{g_m + 4KR_eI_0 \exp\left(\frac{g_bV_{in}^c}{2I_0}\right)} \quad . \tag{4.17}$$

When taking logarithm of both sides, (4.17) becomes

$$20\log|A_v| = 20\log 4I_0KR_eR_dg_m + 10\frac{g_bV_{in}^c}{I_0} - 20\log\left\{g_m + K\left[4I_0\exp\left(\frac{g_bV_{in}^c}{2I_0}\right)\right]\right\}. \tag{4.18}$$

Similar to (4.13), the third term in (4.18) deteriorates the dB linearity. This effect becomes more severe when the input control voltage V_{in}^c is high because in this case, the third term becomes larger. To compensate this effect, the rate of the gain variation versus the control voltage V_{ctrl} when V_{in}^c is high may be purposely made faster than that defined by the exponential function. This is essentially a pre-distortion technique that, to some extent, compensates the nonlinearity introduced by the third term in (4.18). One of possible

implementations of this pre-distortion is to make $I_{CS} > 4I_o$. It can be proved that with such an implementation, the output voltage of the exponential circuit, V_{ctrl}, increases with a faster rate than the ideal exponential one when V_{in}^c is high.

Therefore, the entire circuit including the pseudo-exponential voltage circuit and the compensation is as Fig.4.3.

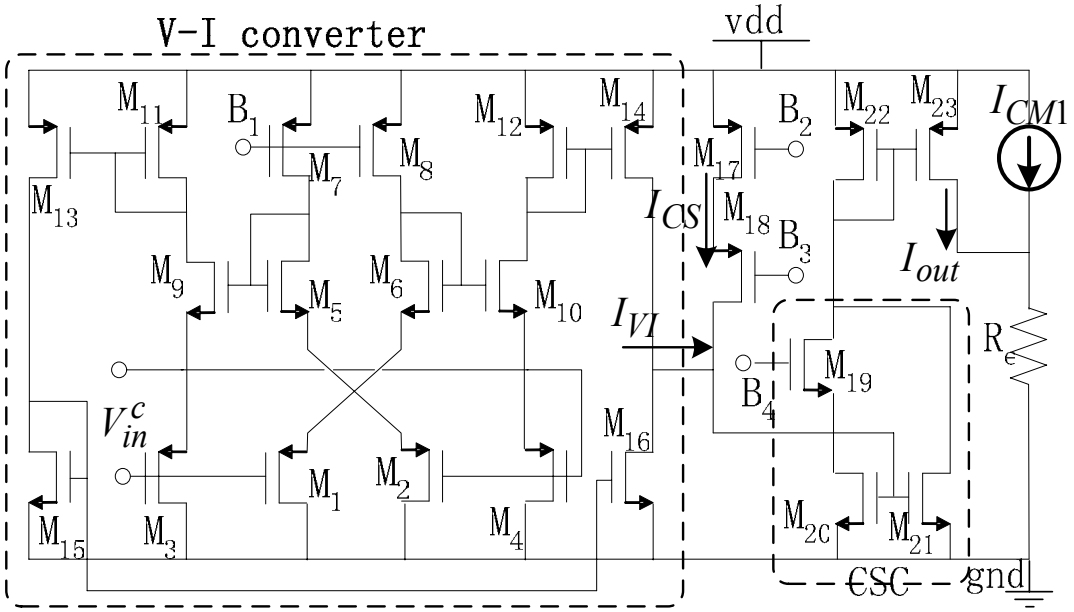


Fig.4.3 Pseudo-exponential voltage circuit with compensation techniques

4.4 Simulation results for dB-linear VGA

This dB-linear VGA is designed in 0.35-μm CMOS technology and simulated with Cadence 4.4.6, HSPICE 2002.2. Fig.4.4 shows the simulation result for the exponential circuit with the pre-distortion technique when I_{CM1} is set to zero. It can be seen that at high input control voltage (V_{in}^c), V_{Ctrl} increases faster than the ideal dB-linear rate. As described in the previous section, this can be used to

compensate the effect of the increased G_s on the overall gain linearity.

Fig.4.5 shows the results of the dB-linear VGA. For the uncompensated VGA (linear VGA + exponential function circuit without dB-linearity compensation), it shows a log-like gain variation with the input control voltage. However, for the compensated VGA (linear VGA + exponential function circuit with dB-linearity compensation), the dB-linearity has been greatly improved and is close to the ideal case. This demonstrates the effectiveness of the proposed compensation techniques.

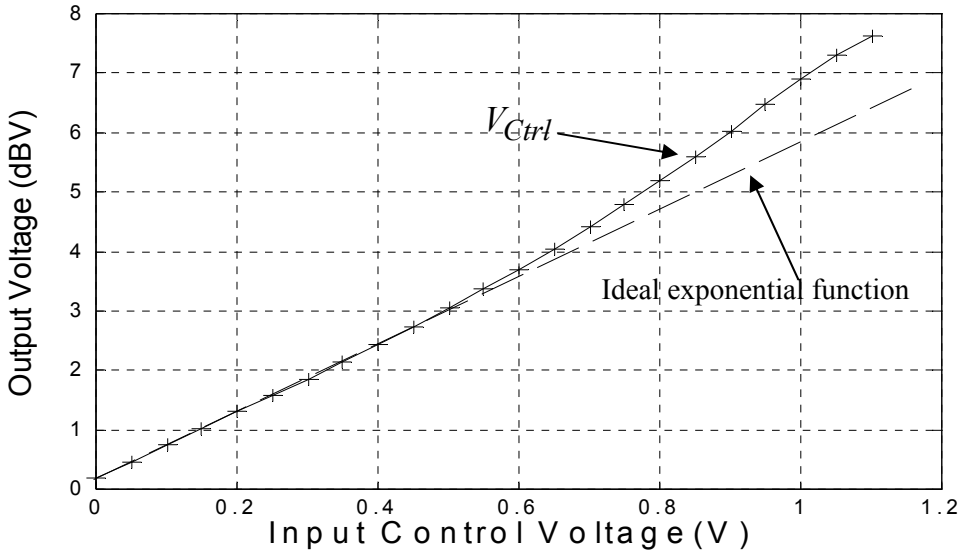


Fig.4.4 Simulation result of the exponential circuit

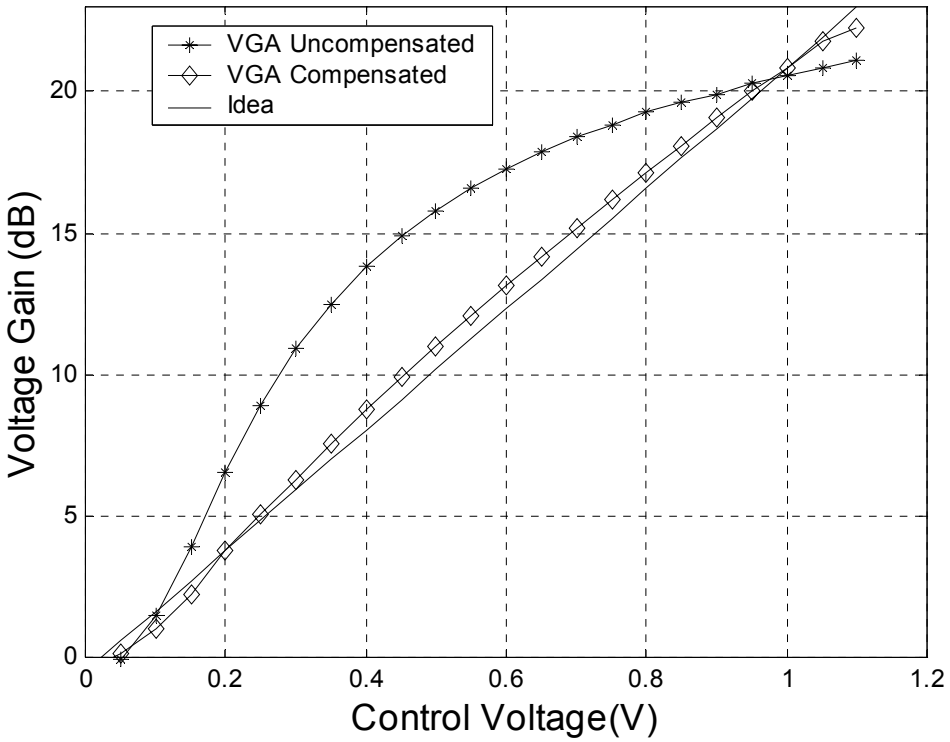


Fig.4.5 Simulation result of the gain of VGA

Chapter 5

A novel DC Offset Cancellation Circuit

The DC offset tuning circuit, shown in Fig.5.1, consists of a buffer and tuning loop. The DC offset sensing and cancellation are performed at the same node, that is, the output of the buffer. The tuning process will be described in details in the following sections.

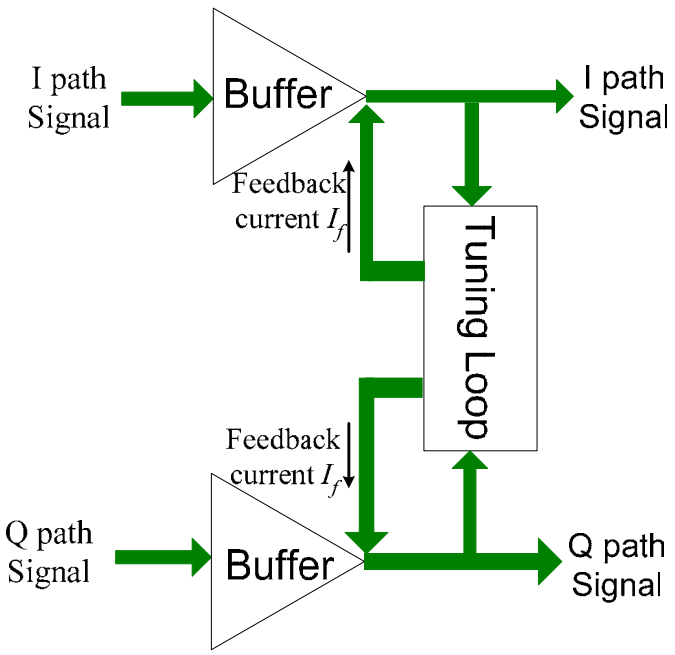


Fig.5.1 DC offset cancellation Circuit

5.1 Buffer in the tuning circuit

The schematic of the buffer is shown in Fig.5.2. It is a linearized transconductance providing unity gain. R_3 is used to improve linearity and adjust the gain of the buffer. The DC offset tuning is performed in current domain through the feedback tuning current and R_1 and R_2. Referring to Fig.5.2, the tuning loop senses the DC offset at the nodes V_{out-} and V_{out+} and neutralize it at the same nodes in the form of feedback tuning current. The DC offset cancellation process is also shown in Fig.5.3.

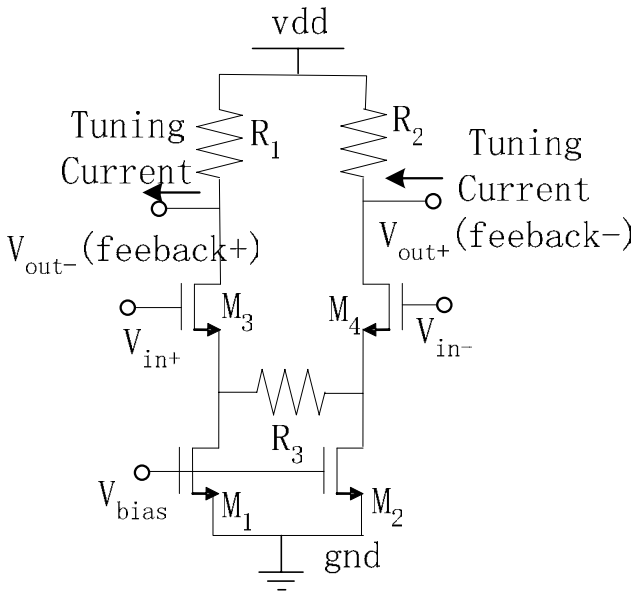


Fig.5.2 The unity gain buffer

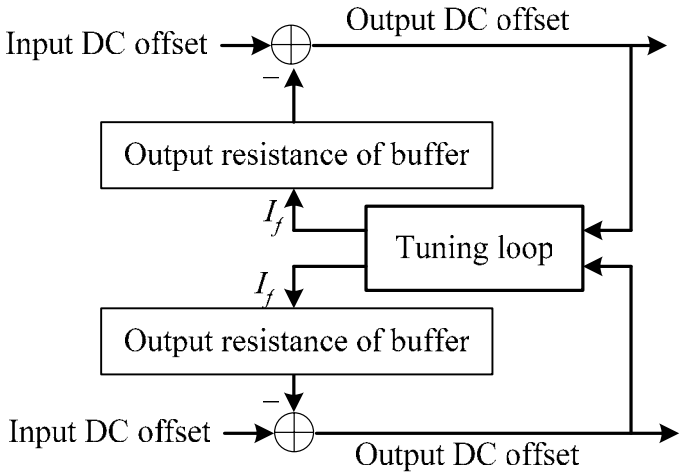


Fig.5.3 DC offset cancellation process in the buffer

5.2 Tuning loop configuration

The proposed DC offset loop is shown in Fig.5.4. It is based on a feedback structure that is similar to the phase-lock loop. A multiplier is used to sense the DC offset embodied in the incoming signals from I and Q path. A Low Pass Filter (LPF) is employed to suppress the residual AC component in the multiplier output and leaves mainly the DC offset. This detected DC offset is then fed to the respective integrator in the I and Q path. The integrator further removes the AC components in the detected signal and accumulates the DC component to provide a DC offset tuning voltage. The tuning voltage is converted to a tuning current I_f (I_{fI} or I_{fQ}) by a V-I converter. The tuning current from the V-I converter is fed back to the buffer and cancels the DC offset. A polarity detection branch, including another LPF and a comparator, is employed in each path to determine the sign of the DC offset so as to switch to tuning signal to the correct branch and ensure a negaive feedback.

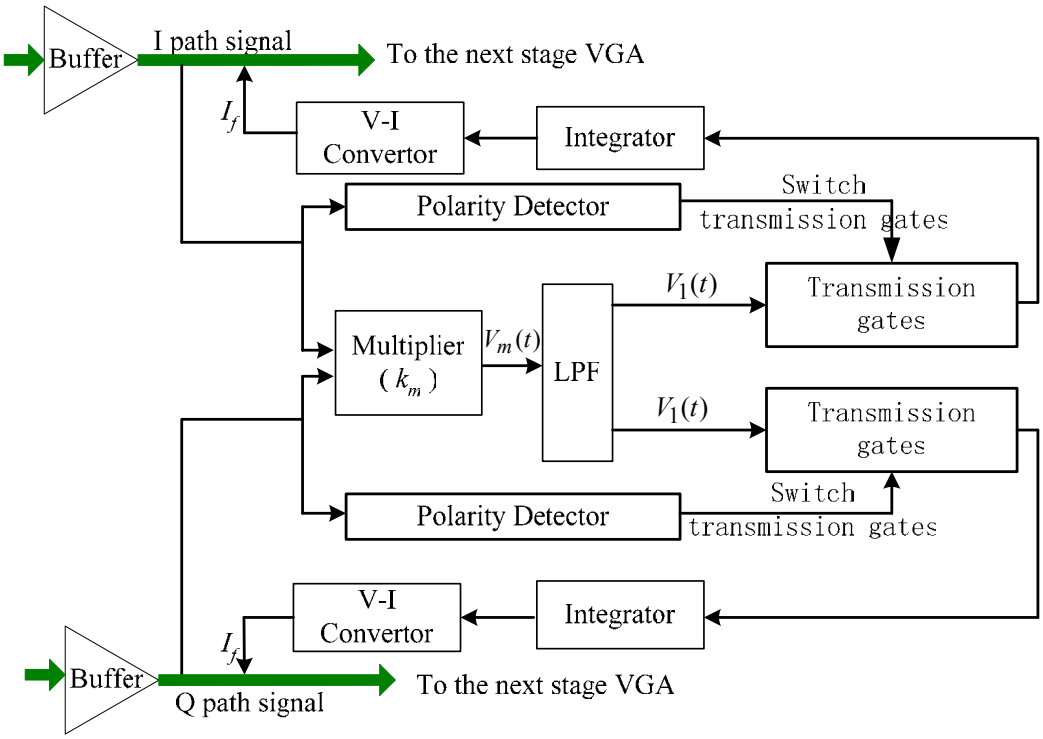


Fig.5.4 Block diagram of Tuning Loop

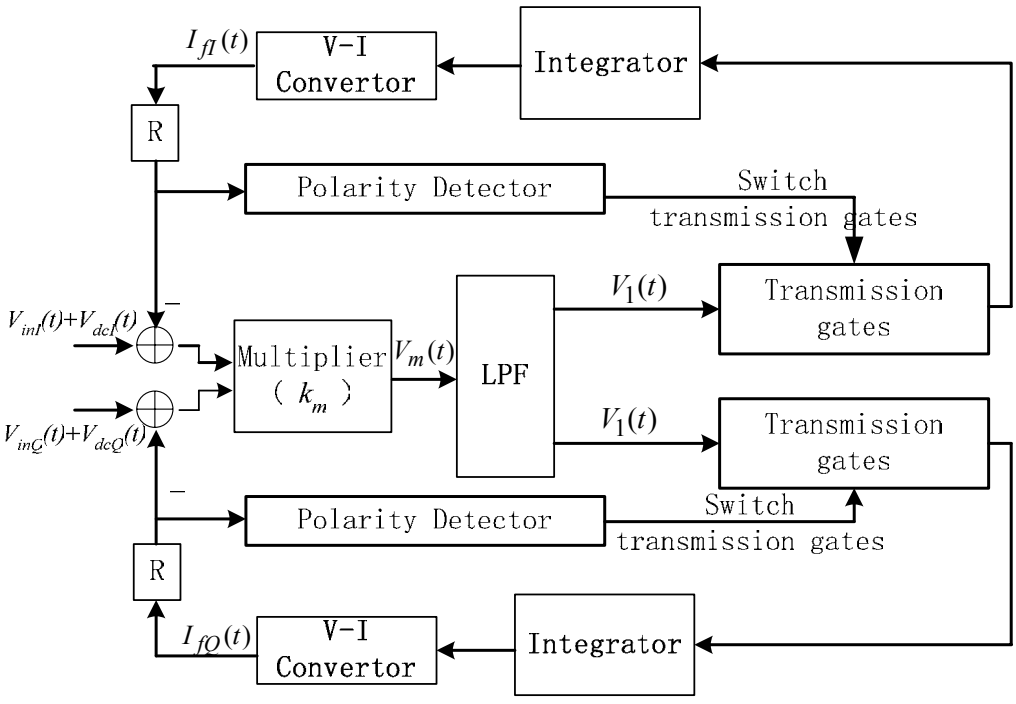


Fig.5.5 DC offset behavior in the DC offset cancellation circuit

Let the DC offset of I and Q path be V_{dcI} and V_{dcQ}, and the input signal of I and Q path are V_{inI} and V_{inQ}, respectively, the output of the multiplier, V_m

$$\begin{aligned} V_m &= k_m \times \left(V_{dcI} + V_{inI}\right) \times \left(V_{dcQ} + V_{inQ}\right) \\ &= k_m \times \left[V_{dcI} \times V_{dcQ} + \left(V_{inI} \times V_{dcQ} + V_{inQ} \times V_{dcI} + V_{inI} \times V_{inQ}\right)\right] \\ &= U + Z. \end{aligned} \tag{5.1}$$

Where k_m denotes the scale factor of the multiplier, and

$$U = k_m \times V_{dcI} \times V_{dcQ} \tag{5.2}$$

$$Z = k_m \times \left(V_{inI} \times V_{dcQ} + V_{inQ} \times V_{dcI} + V_{inI} \times V_{inQ}\right) \tag{5.3}$$

U is a DC signal and Z is a signal including only AC components. The high frequency components of Z will be suppressed by the LPF, and further removed by the integrator. U is integrated to generate the DC offset tuning signal.

After the integration, signal and DC offset becomes

$$V_{inte} = \int V_m dt \tag{5.4}$$

Generally, signals of I and Q path are zero mean and independent. If tuning time is long enough, we arrive at

$$\int V_{inI} dt = 0 \tag{5.5}$$

$$\int V_{inQ} dt = 0 \tag{5.6}$$

$$\int \left(V_{inI} \times V_{inQ} \right) dt = 0 \tag{5.7}$$

Thus V_{inte} is

$$\begin{aligned} V_{inte} &= \int U dt + \int Z dt \\ &= k_m \int \left(V_{dcI} \times V_{dcQ} \right) dt + k_m \int \left(V_{inI} \times V_{dcQ} + V_{inQ} \times V_{dcI} + V_{inI} \times V_{inQ} \right) dt \\ &= k_m \int \left(V_{dcI} \times V_{dcQ} \right) dt + k_m V_{dcQ} \int V_{inI} dt + k_m V_{dcI} \int V_{inQ} dt + k_m \int \left(V_{inI} \times V_{inQ} \right) dt \end{aligned} \tag{5.8}$$

From (5.5)-(5.7), we can arrive at

$$V_{inte} = k_m \int \left(V_{dcI} \times V_{dcQ} \right) dt \tag{5.9}$$

As a result, even some low frequency components of Z that are not removed by the LPF, will be removed by the integrator. Therefore, requirement of LPF is greatly softened.

5.3 DC offset detection issues

The proposed DC offset detection scheme using a multiplier and an LPF has some merits, but it may have some potential problems under certain circumstances.

First, positive feedback may occur due to the unrecognizable polarity of the DC offset. To ensure negative feedback of the tuning loop, the following

inequalities should be satisfied

$$V_{dcI} \times I_{fI} < 0 \tag{5.10}$$

and

$$V_{dcQ} \times I_{fQ} < 0 \tag{5.11}$$

But since the source of the feedback signal U is the product of V_{dcI} and V_{dcQ}, in some cases, (5.10)-(5.11) may not stand. For example, when both V_{dcI} and V_{dcQ} change their polarity concurrently, U keeps its polarity unchanged. In this case, $V_{dcI} \times I_{fI} > 0$ and positive feedback occurs. Hence polarity detection branches are needed to maintain a negative feedback loop.

The interaction among the polarity related quantities is listed in Table I. The values of $sign(\bullet)$ represent positive (1) or negative (0) polarity respectively. The values of PI (PQ) represent that the tuning voltage of I (Q) path is subtracted from (1) or added to the signal.

Table 2 Decision for tuning direction

$sign(V_{dcI})$	$sign(V_{dcQ})$	$sign(U)$	PI	PQ
0	0	1	0	0
0	1	0	1	0
1	0	0	0	1
1	1	1	1	1

From Table 2, it can be deduced that $\mathrm{PI} = \overline{sign(V_{dcI}) \oplus sign(U)}$ and $\mathrm{PQ} = \overline{sign(V_{dcQ}) \oplus sign(U)}$. After simplification, we can arrive, $\mathrm{PI} = sign(V_{dcQ})$ and $\mathrm{PQ} = sign(V_{dcI})$. This implies that the polarity control signal of the

transmission gate in I (Q) path comes from the output of comparator in Q (I) path.

Based on the above analysis, the polarity decision branch is implemented by an LPF_P, a comparator, and transmission gates, as shown in Fig.5.6. The LPF_P is to obtain the desired DC component, V_{1I} and V_{1Q}, so that the comparator can decide the polarity of the DC offset. Control signals of transmission gates are cross connected, that is, the output of comparator in I path controls the transmission gates in the Q path, and vice versa.

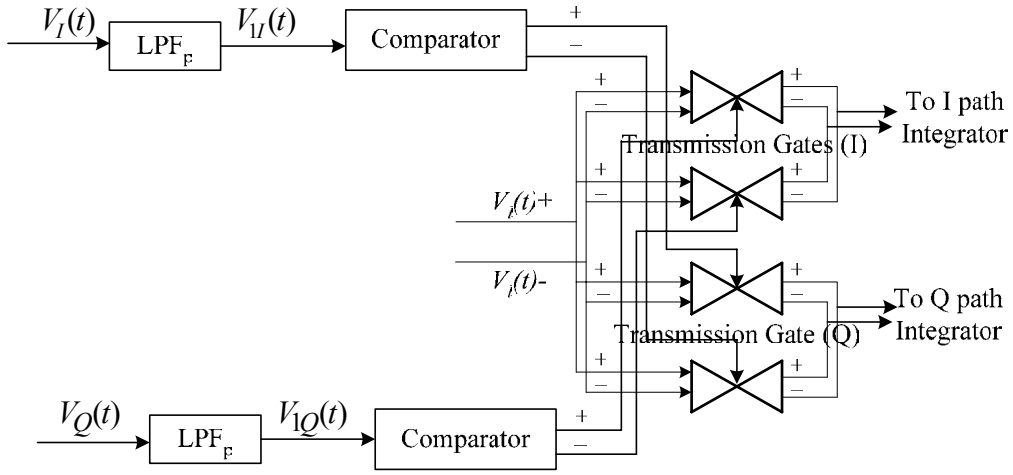


Fig.5.6 Polarity Decision Branch

Secondly, insufficient phase margin may occur and cause instability. As mentioned above, U becomes an extremely large value as DC offset increases. This may cause such a high open loop gain and insufficient phase margin. To ensure the loop stability, a limiter is employed after the multiplier. The output of the limiter is constrained within a moderate range, so is the loop gain. If the loop works properly in its most hostile situation, the highest open loop gain mode, it

will also work stably in a lower gain mode which has larger phase margin.

5.4 I/Q Mismatch Issues

I/Q mismatch is unavoidable in a fabricated chip, and it will affect the tuning result. When mismatch exists, either V_{dcI} or V_{dcQ} will be tuned to zero firstly. If anyone of V_{dcI} and V_{dcQ} is zero, the integrator input, *U*, becomes zero. In this case, the tuning ceases even though DC offset still exists in the other path. Combination tuning scheme is used to solve this problem. The modified scheme is to use a summation block to use the combination of the output of the multiplier V_m, DC offset of I path V_{1I}, and DC offset of Q path V_{1Q}, as the input to the integrator, which can be written as

$$\begin{aligned} V_{sum} &= k_2 \times V_m + k_{1I} \times V_{1I} + k_{1Q} \times V_{1Q} \\ &= k_2 k_m \times V_{dcI} \times V_{dcQ} + k_{1I} \times V_{1I} + k_{1Q} \times V_{1Q} \end{aligned} \tag{5.12}$$

where k_2, k_{1I}, k_{1Q}, denotes the weights of each component. Here V_{1I} and V_{1Q} come from the polarity decision branch, which need not be critical DC voltages because the AC components will be further removed by the integrator. k_2 is chosen to be much larger than k_{1I} and k_{1Q} so that the new introduced items $k_{1I} \times V_{1I}$ and $k_{1Q} \times V_{1Q}$ will not affect the stability and the negative feedback of the tuning loop. In the modified scheme, V_{sum} will become zero if and only if both V_{dcI} and V_{dcQ} are zero. If V_{sum} does become zero, subsequently, tuning loop will be locked. Therefore, according to (5.12), the tuning loop can cancel the

DC offset and suppress effects of I/Q mismatch due to DC offset simultaneously. Because the requirement for V_{1I} and V_{1Q} to be DC voltage is not critical, the output of LPF_P can be used as V_{1I} and V_{1Q}.

The block diagram of the final tuning loop is shown in Fig.5.7.

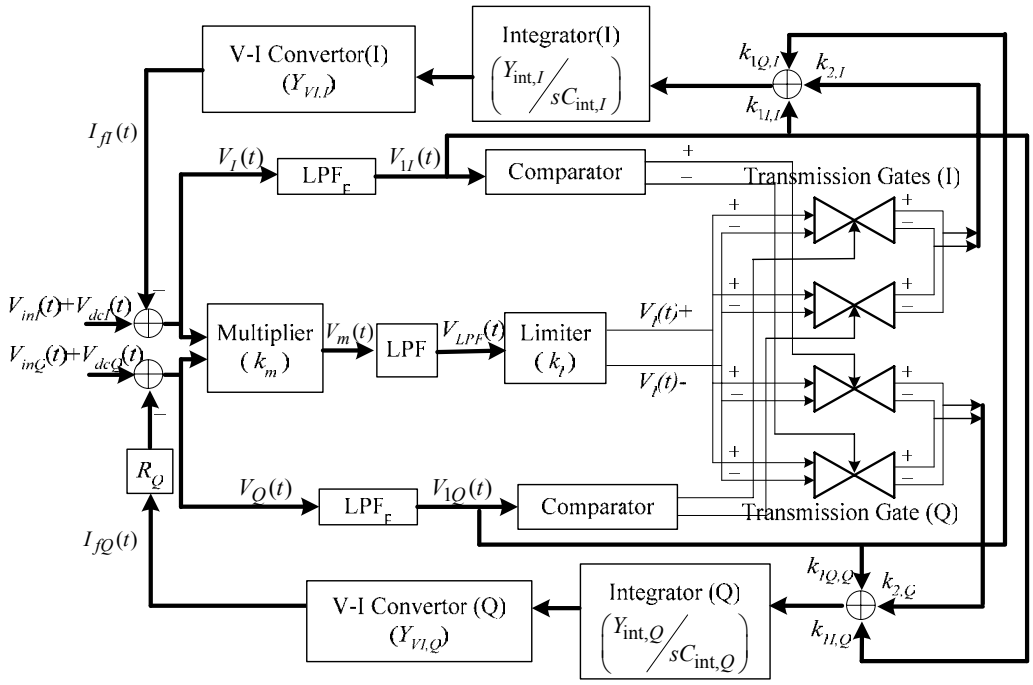


Fig.5.7 Entire Diagram of the Tuning Loop

5.5 Circuit Implementation

5.5.1 Multiplier

The DC offset tuning loop can be fully integrated without any external components. In the proposed implementation, the multiplier shown in Fig.5.8 is designed based on the one in [69]. The output can be written as:

$$\begin{aligned} V_{out} &= \left(-32R_bK_bR_a^2K_a^2\left(V_{in1}-V_{th}\right)\left(V_{in2}-V_{th}\right)\right)V_{in1}V_{in2} \\ &= k_mV_{in1}V_{in2} \end{aligned} \tag{5.13}$$

where $K = \frac{1}{2}\mu_n c_{ox}\left(\frac{W}{L}\right)$ is the transconductance parameter. In our design, all MOSFET's M_{ai} (M_{bi}) are identical with the same K_a (K_b). The values of the resistors R_{ai} (R_{bi}), i=1-4, is R_a (R_b). V_{th} denotes the threshold voltage. Therefore, the scale factor k_m can be determined by the transistor size, the resistor value, and the common mode of the input signal [69]. To achieve high sensitivity, k_m should have a large value.

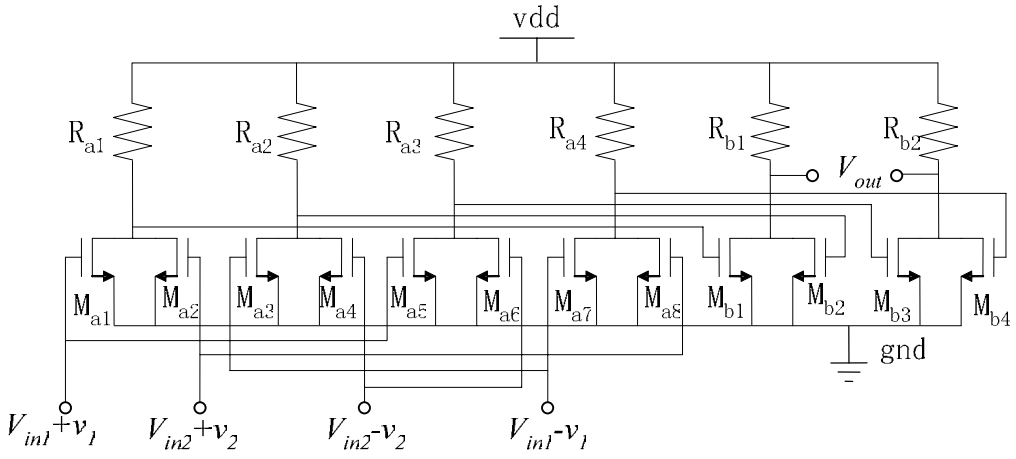


Fig.5.8 Schematic of the Multiplier

5.5.2 Low Pass Filter

The active gm-C low pass filter is shown in Fig.5.9. M_5 and M_6 form the linear transconductor with common mode feedback circuit consisting of M_9-M_{13}. M_7 and M_8 are the active loads with an equivalent resistance R_L, which can be expressed as $1/\lambda I_b$. Here λ is the channel length modulation coefficient and I_b is the bias current of the LPF. Therefore, with an on chip capacitor C_L, the cutoff

frequency of the g_m-C LPF can be expressed as

$$\begin{aligned}\omega_{LPF} &= \frac{1}{R_L C_L} \\ &= \frac{\lambda I_b}{C_L}\end{aligned} \tag{5.14}$$

Our design shows that a low cutoff frequency of 10 kHz can be realized with an on-chip capacitance of 3 pF.

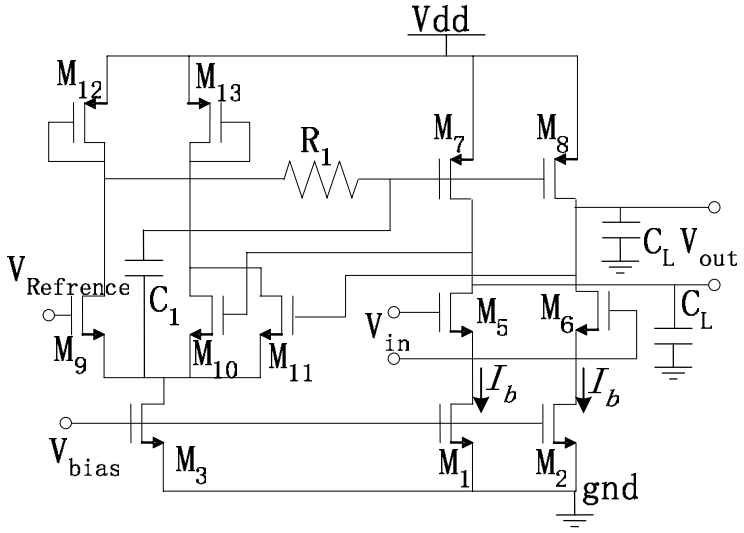


Fig.5.9 Schematic of the LPF

5.5.3 Integrator and V-I convertor

The differential gm-C integrator is shown in Fig.5.10. The gm cell is formed by transistors M_1–M_{20} [67], together with an on-chip capacitor C_{int}. Similar circuit is used to implement the V-I convertor, shown in Fig.5.11. To accommodate the common mode output voltage from the Integrator, which can be as low as 0.5 V, PMOS transistors are used as the input stage.

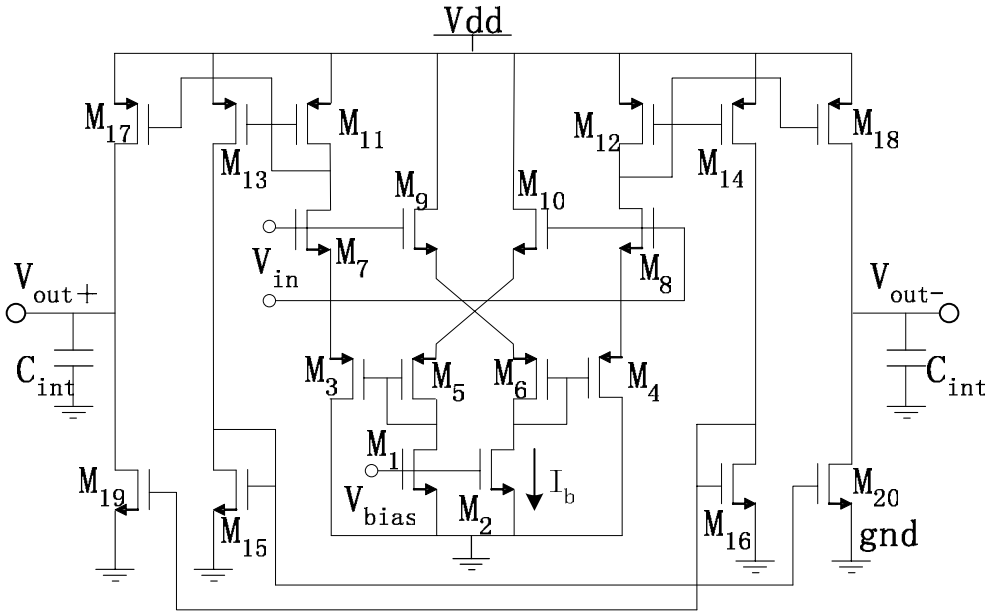


Fig.5.10 Schematic of Integrator

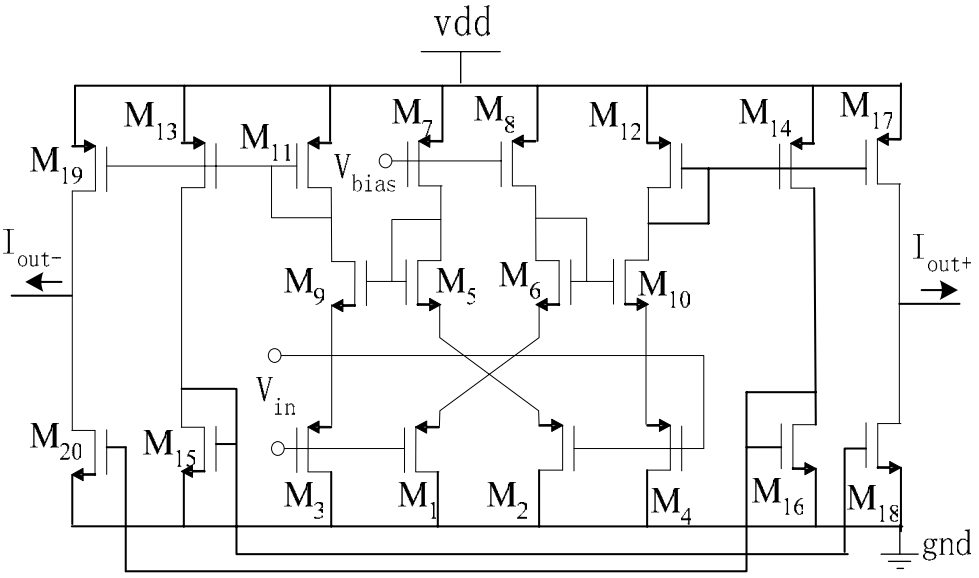


Fig.5.11 Schematic of the V-I converter

5.5.4 Comparator

The comparator for DC offset polarity decision is designed based on [70]. The schematic of this comparator is shown in Fig.5.12. M_1-M_6 form a high gain amplifier. The gain of this amplifier can be written as:

$$A_{comp} = g_{m1} \times \left(\frac{1}{g_{m3}} - \frac{1}{g_{m6}} \right) \tag{5.15}$$

Where $g_{m1,}$ g_{m3} and g_{m6} represent the transconductance of M1 (M2), M3 (M4) and M6 (M5) respectively. High gain can be achieved by choosing g_{m3} and g_{m6} close to one another. However, if g_{m6} is greater than g_{m3}, that is:

$$\frac{1}{g_{m3}} < \frac{1}{g_{m6}} \tag{5.16}$$

It is no longer high gain amplifier. M_1-M_6 work with M_7-M_{11} to form the comparator.

To get the inverted output, an inverter formed by M_{12} and M_{13} is used after the comparator. Because the delay introduced by the inverter is about tens nano-seconds, which is mush faster than the changes of DC offset, the inverter will not affect the decision of the comparator.

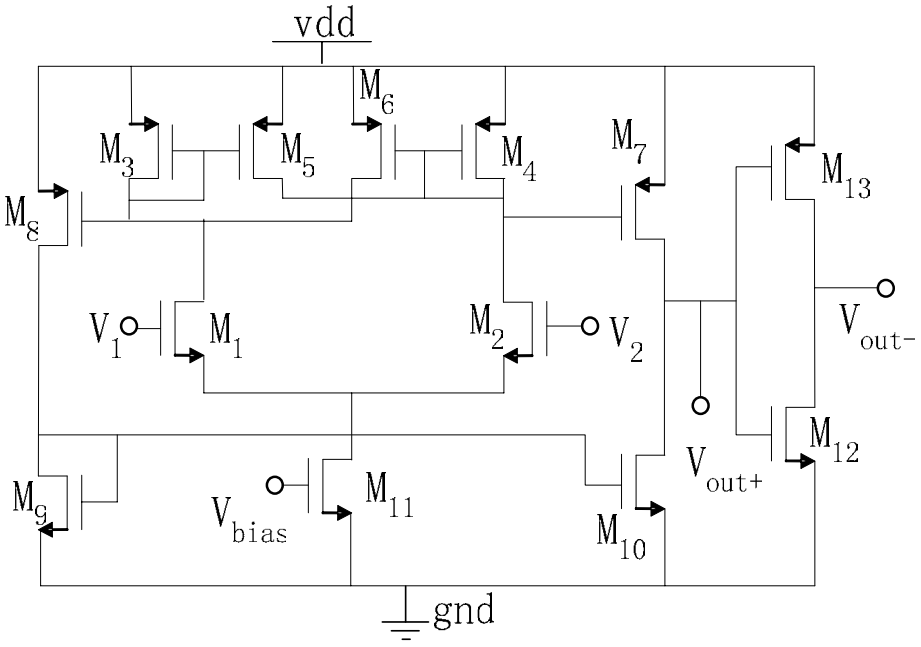


Fig.5.12 Schematic of Comparator

5.5.5 Limiter and summation block

Schematic of the limiter is shown in Fig.5.13. M_3 and M_4 is the differential pair. R_2 and R_3 are output resistance. R_1 is used to improve linearity and adjust the gain of the limiter. R_4 is employed to limit the highest voltage level of the output. The highest and lowest voltage level of the output can be determined by:

$$V_{high} = \mathrm{vdd} - 2\mathrm{I}_{\mathrm{bias}}\mathrm{R}_4 \tag{5.17}$$

$$V_{low} = \mathrm{vdd} - 2\mathrm{I}_{\mathrm{bias}}\mathrm{R}_4 - 2\mathrm{I}_{\mathrm{bias}}\mathrm{R}_2 \tag{5.18}$$

Where I_{bias} is the bias current. Thus appropriate range of the limited level, and the common mode of the output can be decided by R_2/R_3, R_4 and I_{bias}.

Summation block is used to suppress I/Q mismatch. Schematic of the

summation block is shown in Fig.5.14. M_3 & M_4, M_6 & M_7 and M_9 & M_{10} are three differential transconductance pairs that convert the input voltage to current. The currents are summed by R_1 and R_2. M_3 & M_4 and M_6 & M_7 have equal size and equal bias current, while the bias current of M_9 and M_{10} is much higher. Refer to section 5.4 (5.13), by this bias current distribution, the weight of V_{1I} and V_{1Q}, (k_{1I} and k_{1Q}) in the summation is much less than $V_{dcI} \times V_{dcQ}$ and $k_{1I} = k_{1Q}$. This ensure that $k_{1I}V_{1I}$ and $k_{1Q}V_{1Q}$ will not affect the stability of the tuning loop.

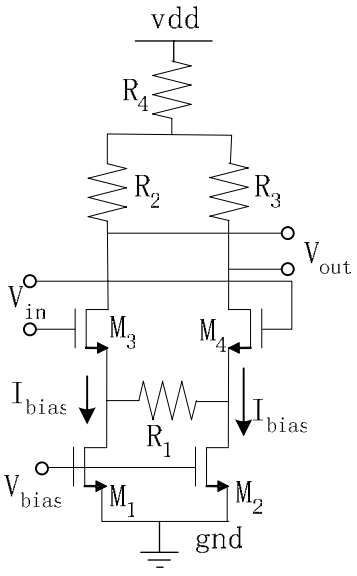


Fig.5.13 Schematic of Limiter

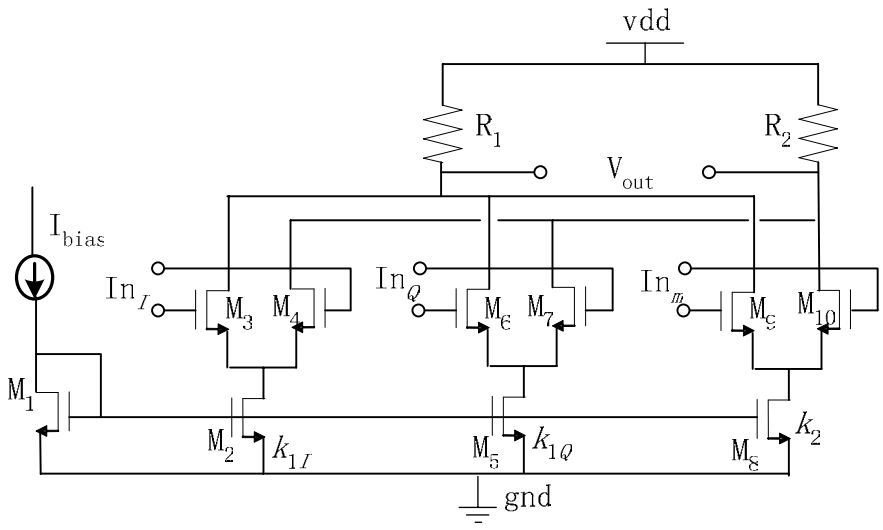


Fig.5.14 Schematic of the summation block

5.6 Adaptive Bandwidth Varying

Loop settling time is an important parameter. The settling time of the tuning loop is closely related to ω_{LPF}, the cutoff frequency of LPF. The larger the ω_{LPF}, the quicker the settling rate [71]. However, in the DC offset tuning loop for DCR architecture, ω_{LPF} can not be too large because the frequency response of the close loop is a high pass filter characteristic, and an excessively large ω_{LPF} will lead to corruption of desired signal. Therefore, there is a trade off between settling time and maintaining desired signal when choosing ω_{LPF}.

To overcome this problem, a varying ω_{LPF} loop is employed. Since in DCRs, the VGA needs some time to adjust its gain to an appropriate level. During this period, the performance of signal demodulation will be degraded. Hence, within this time period, large ω_{LPF} can be used to accelerate the DC offset tuning. With DC offset being suppressed ω_{LPF} is decreased adaptively. When the VGA has

switched to the proper gain mode, ω_{LPF} becomes small enough so that it removes only DC offset and will not affect the desired signal. ω_{LPF} can be changed by adaptively adjusting the bias current applied to the LPF. Referring to Fig.5.15, when a step signal $V_c u(t)$ occurs at V_2, and if the initial value of V_p is V_0, $V_p(t)$ can be represented as

$$V_p(t) = (V_0 - V_c)e^{-t/RC} + V_c. \tag{5.19}$$

where V_c can be given once the receiver is power on. Accordingly, the drain current of M_1 is

$$\begin{aligned} I_1 &= \frac{1}{2}\mu_n C_{ox}\left(W/L\right)\left(\mathrm{Vdd} - V_p - \left|V_{thp}\right|\right)^2 \\ &= \eta\left(\mathrm{Vdd} - V_p - \left|V_{thp}\right|\right)^2 \end{aligned} \tag{5.20}$$

where $K = \mu_n C_{ox}(W/L)$. I_1 is mirrored to serve as the bias current of LPF, $I_b = k_b I_1$, where k_b denotes the gain of the current mirror. Together with (5.20), the relationship of ω_{LPF}, and R and C can be expressed as

$$\begin{aligned} \omega_{LPF}(t) &= \frac{\lambda k_b \eta\left(\mathrm{Vdd} - V_p - \left|V_{thp}\right|\right)^2}{C_L} \\ &= \frac{\lambda k_b \eta}{C_L}\left(\mathrm{Vdd} - (V_0 - V_c)e^{-t/RC} - V_c - \left|V_{thp}\right|\right)^2. \end{aligned} \tag{5.21}$$

Generally, the initial value of V_1 can be set to 0, eg. S1 is shut down during initial state, $V_0 = 0$, and V_C can be given as Vdd. Therefore, (5.21) can be written

as

$$\omega_{LPF}(t)=\frac{\lambda k_b \eta}{C_L}\left(\mathrm{Vdd}\cdot e^{-t/RC}+\left|V_{thp}\right|\right)^2. \tag{5.22}$$

With the appropriate value of *R* and *C*, the ω_{LPF} can be increased during the start-up and hence improves the settling time.

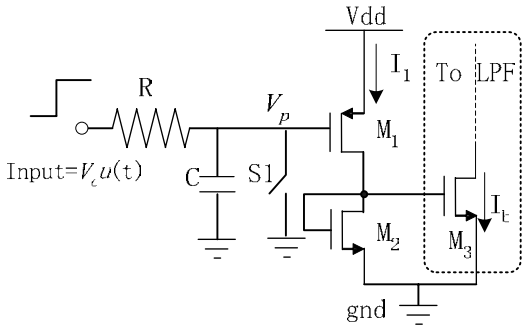


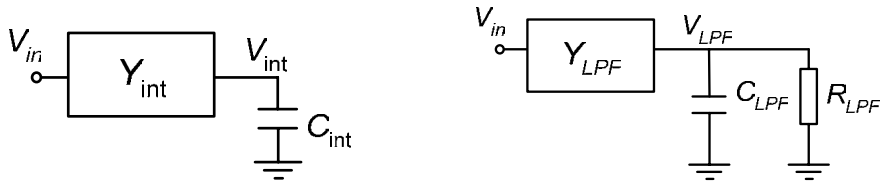
Fig.5.15 Implementation of Bandwidth varying

5.7 Large signal analysis (Transient Analysis)

5.7.1 Large signal analysis derivation

To find the large signal transient response of the tuning loop mathematically, we use differential equations to describe the tuning loop.

The diagram of integrator and LPF is shown in Fig. 5.16.



(a) Diagram of Integrator (b) Diagram of LPF

Fig.5.16 Equivalent model of the integrator and LPF

$$Y_{\text{int}}V_{in} = C_{\text{int}}\frac{dV_{\text{int}}}{dt} \tag{5.23}$$

$$V_{\text{int}} = \frac{Y_{\text{int}}}{C_{\text{int}}}\int V_{in}dt \tag{5.24}$$

$$Y_{LPF}V_{in} = \frac{V_{LPF}}{R_{LPF}} + C_{LPF}\frac{dV_{LPF}}{dt} \tag{5.25}$$

With the equations describing LPF and integrator, the tuning loop can be described by (5.26)-(5.30). Here, V_{inI} (V_{inQ}) and V_I (V_Q) are the input and output signal of I (Q) path. R_I and R_Q denotes the output resistor of buffer in I path and Q path respectively. C_{1I} (C_{1Q}), Y_{1I} (Y_{1Q}), and R_{1I} (R_{1Q}) denote the capacitance, the transconductance and the output resistance of the LPF_P in I (Q) path. For $C_{\text{int\_}I}$ ($C_{\text{int\_}Q}$), Y_{VI_I} (Y_{VI_Q}) and $Y_{\text{int\_}I}$ ($Y_{\text{int\_}Q}$), the first subscript denotes the function block and the second one after the underline denotes it is in the I (Q) path. Other symbols have been defined before.

$$\begin{aligned} V_I(t) = V_{inI}(t) + V_{dcI}(t) - R_I Y_{VI\_I}\frac{Y_{\text{int\_}I}}{C_{\text{int\_}I}}\times \\ \int\left[k_{1I\_I}V_{1I}(t) + k_{1Q\_I}V_{1Q}(t) + k_{2\_I}k_l sign\left(V_Q(t)\right)V_{LPF}(t)\right]dt \end{aligned} \tag{5.26}$$

$$V_Q(t) = V_{inQ}(t) + V_{dcQ}(t) - R_Q Y_{VI\_Q} \frac{Y_{\text{int}\_Q}}{C_{\text{int}\_Q}} \times \int \left[k_{1I\_Q} V_{1I}(t) + k_{1Q\_Q} V_{1Q}(t) + k_{2\_Q} k_l sign\left(V_I(t)\right) V_{LPF}(t) \right] dt \tag{5.27}$$

$$\frac{V_{1I}(t)}{R_{1I}} + C_{1I} \frac{dV_{1I}(t)}{dt} = Y_{1I} V_1(t) \tag{5.28}$$

$$\frac{V_{1Q}(t)}{R_{1Q}} + C_{1Q} \frac{dV_{1Q}(t)}{dt} = Y_{1Q} V_Q(t) \tag{5.29}$$

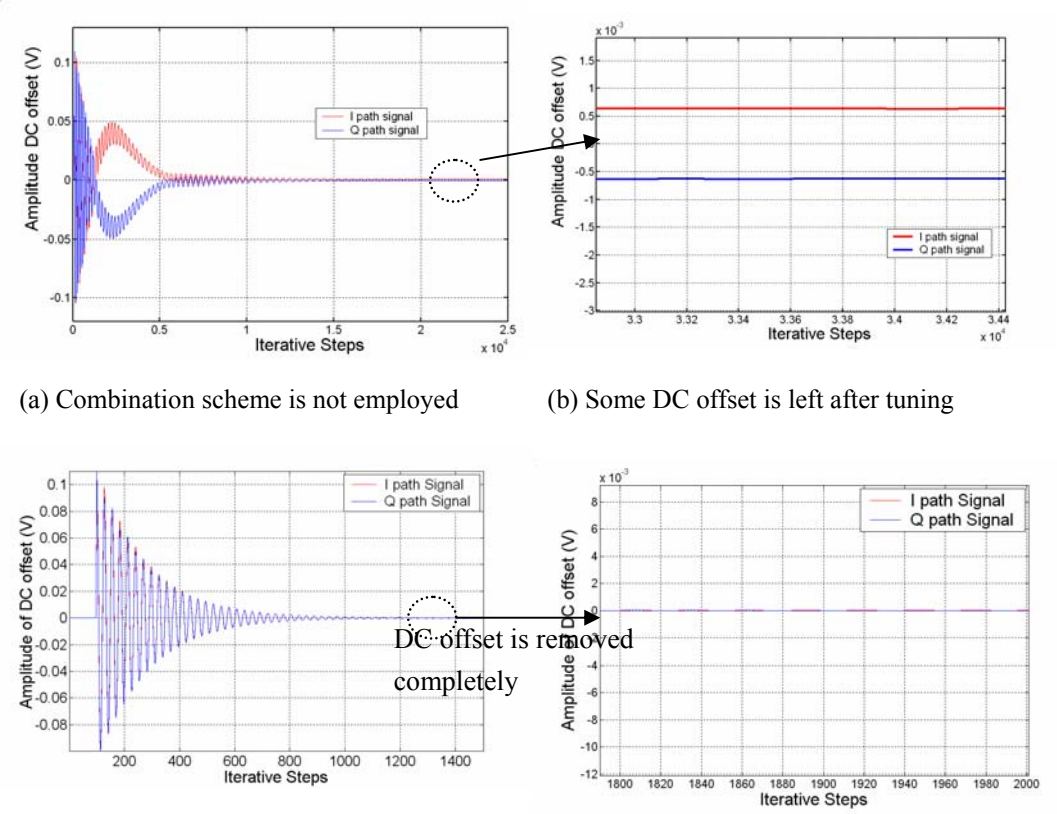
$$k_m Y_{LPF} V_I(t) V_Q(t) = \frac{V_1(t)}{R_{LPF}} + C_{LPF} \frac{dV_1(t)}{dt} \tag{5.30}$$

(5.26) and (5.27) describe the signal path of the tuning loop of I and Q path. (5.28) and (5.290) describe the behavior of LPF_P of I and Q path respectively. And (5.30) describes the behavior of the LPF after the multiplier.

5.7.2 MATLAB simulation for large signal analysis

Equation (5.26) to (5.30) is solved by MATLAB to describe the DC offset tuning behavior. Trapezoidal rule is used to obtain the numerical solution of the differential equations. Trapezoidal rule is a third order operator and can ensure that the approximation has sufficient accuracy. Fig.5.17 shows the MATLAB simulation results when I/Q mismatch exists. Fig.5.17 (a) and (b) is the result when combination tuning scheme is not employed. It can be seen that when I/Q mismatch exists, the DC offset can not be removed completely (Fig.6.1 (b)). While when combination scheme is employed, DC offset can be removed

completely, the cancellation is not affected by I/Q mismatch (Fig.5.17 (d)).



(a) Combination scheme is not employed

(b) Some DC offset is left after tuning

(c) Combination scheme is employed

(d) DC offset can be removed effectively

Fig.5.17 MATLAB Simulation of DC offset tuning for combination tuning scheme to suppress I/Q mismatch effect

Varying bandwidth loop and fixed bandwidth loop are simulated separately to investigate their effects on the settling time. The simulated results are shown in Fig.5.18. DC offset is introduced at n=100. In both case, the tuning loop can remove DC offset even when 10% I/Q mismatch is present. However the loop settles much faster when varying bandwidth technique is applied. The results also shows that this tuning loop can suppress the DC offset and I/Q mismatch due to DC offset simultaneously.

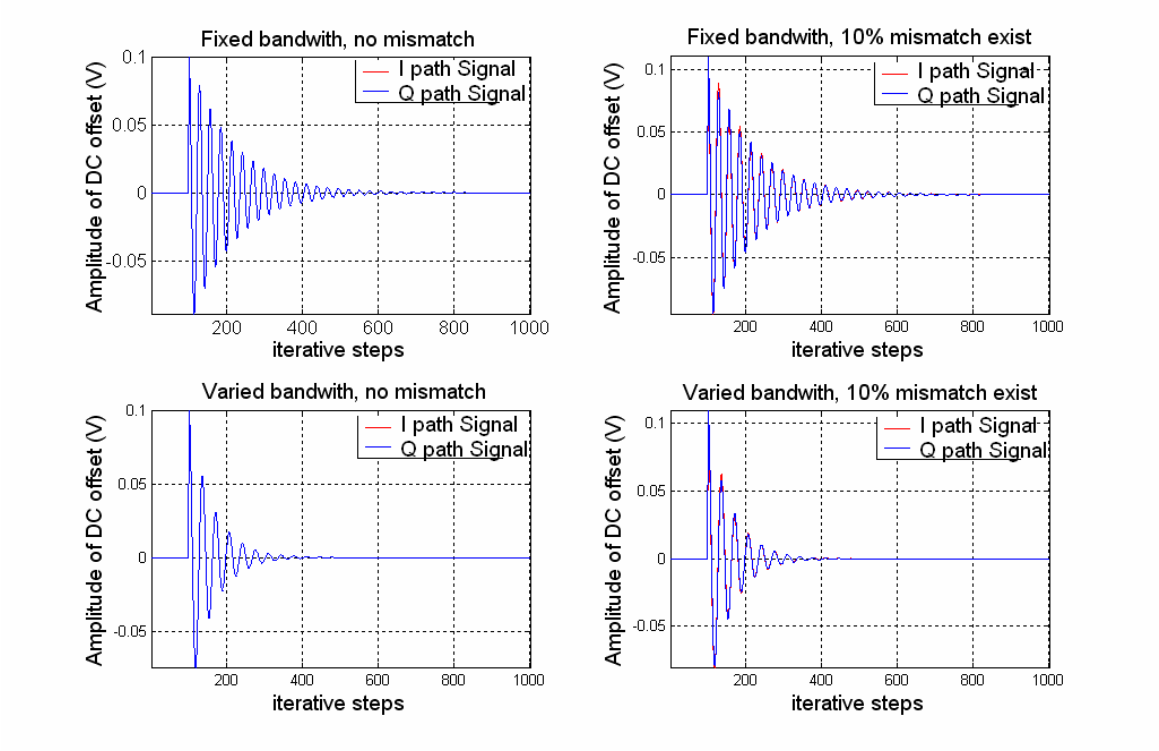


Fig.5.18 MATLAB Simulation of DC offset tuning for varying bandwidth and fixed bandwidth

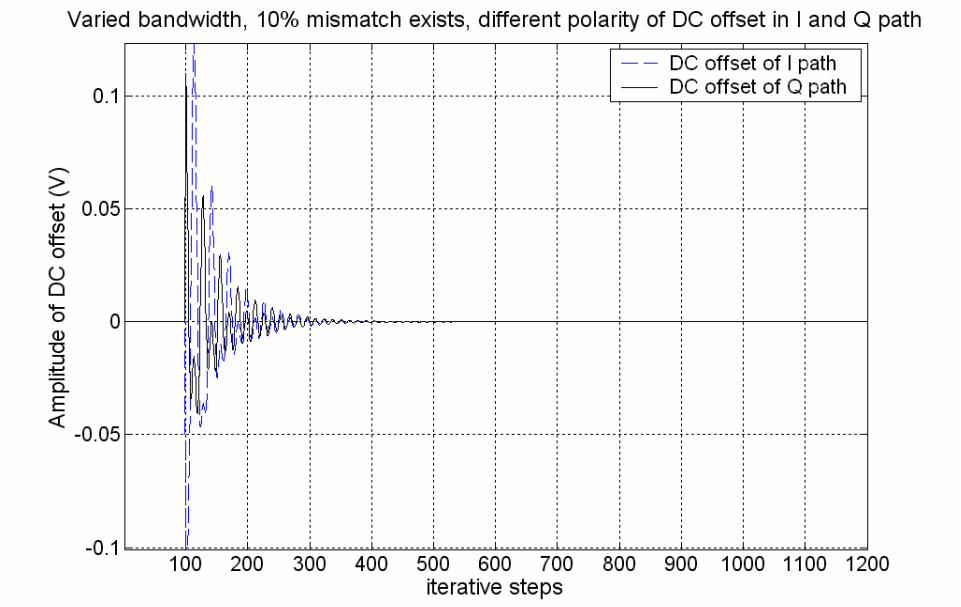


Fig.5.19 MATLAB Simulation of DC offset tuning for I, Q DC offset with different polarity

DC offset of I and Q path with different polarity is presented in the simulation. The result is shown in Fig.5.19. It can be seen that the tuning process does not

affected by different polarity. This validates the cross connection scheme employed in the polarity decision.

5.8 Small signal analysis (Steady state analysis)

Although the DC offset tuning is applied to both I and Q path. For simplicity, only one loop (I or Q) is used for steady state analysis. The linearized feedback tuning system of one loop is shown in Fig.5.20.

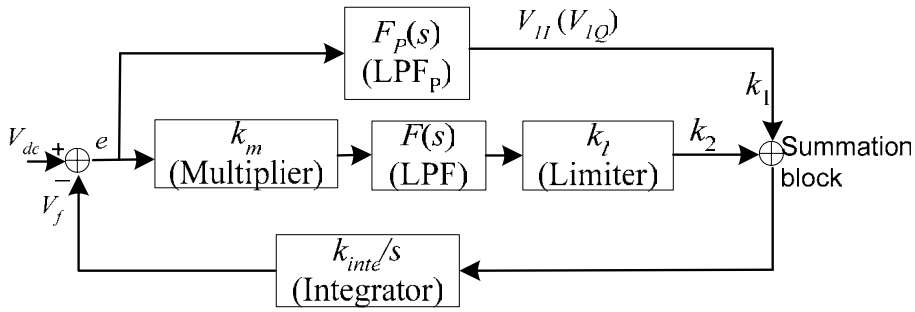


Fig.5.20 Linearized model of DC offset tuning loop

The LPF$_P$ used in Fig.5.20 is used to generate V_{II} or V_{IQ} which is a part of the summation block.

Assuming that V_{dc} represents the DC offset introduced to the tuning loop and a first-order loop filter is used, that is

$$F(s)=\frac{g_m R_L}{1+\dfrac{s}{\omega_{LPF}}}. \tag{5.31}$$

where $g_m R_L$ is the DC gain of the loop filter. Assuming the output of the LPF is not too large so that the limiter can be regarded as an amplifier. Similarly, using a

first-order filer in the polarity decision branch, transfer function of LPF_P can be written as

$$F_P(s) = \frac{g_{mP}R_{LP}}{1+\frac{s}{\omega_{LPFP}}}. \tag{5.32}$$

When the loop is in the vicinity of the steady state, the DC offset has been tuned to be a constant value so as the gain of the multiplier. Based on these assumptions, the close loop transfer function of the loop can expressed as

$$V_f(s) = \left(V_{dc}(s) - V_f(s)\right)\left(k_m F(s) k_l k_2 + F_P(s) k_1\right)\frac{k_{inte}}{s} \tag{5.33}$$

$$V_f(s) = \frac{\left(k_m F(s) k_l k_2 + F_P(s) k_1\right)\frac{k_{inte}}{s}}{1+\left(k_m F(s) k_l k_2 + F_P(s) k_1\right)\frac{k_{inte}}{s}} V_{dc}(s) \tag{5.34}$$

Therefore, $e(s)$ can be written as:

$$\begin{aligned} e(s) &= V_{dc}(s) - V_f(s) \\ &= \frac{1}{1+\left(k_m F(s) k_l k_2 + F_P(s) k_1\right)\frac{k_{inte}}{s}} V_{dc}(s) \end{aligned} \tag{5.35}$$

Substituting (5.28) and (5.29) into (5.32), yield

$$\frac{e}{V_{dc}}(s)=\frac{1}{1+\left(k_m k_l k_2 \frac{g_m R_L}{1+\frac{s}{\omega_{LPF}}}+k_1 \frac{g_{mP} R_{LP}}{1+\frac{s}{\omega_{LPFP}}}\right)\frac{k_{inte}}{s}} \tag{5.36}$$

$$=\frac{s\left(1+\frac{s}{\omega_{LPF}}\right)\left(1+\frac{s}{\omega_{LPFP}}\right)}{s\left(1+\frac{s}{\omega_{LPF}}\right)\left(1+\frac{s}{\omega_{LPFP}}\right)+A_1\left(1+\frac{s}{\omega_{LPFP}}\right)+A_2\left(1+\frac{s}{\omega_{LPF}}\right)}$$

Where $A_1 = k_m k_l k_{inte} g_m R_L$, $A_2 = k_{inte} k_1 g_{mP} R_{LP}$, denotes the loop gain. A reasonable assumption is that $V_{dc}(0)$ is bounded by a finite value, thus

$$\lim_{t\to\infty} e(t) = \lim_{s\to 0} se(s)$$

$$=\lim_{s\to 0} s\frac{s\left(1+\frac{s}{\omega_{LPF}}\right)\left(1+\frac{s}{\omega_{LPFP}}\right)}{s\left(1+\frac{s}{\omega_{LPF}}\right)\left(1+\frac{s}{\omega_{LPFP}}\right)+A_1\left(1+\frac{s}{\omega_{LPFP}}\right)+A_2\left(1+\frac{s}{\omega_{LPF}}\right)}V_{dc}(s).$$

(5.37)

Typically the DC offset is a step signal, $V_{dc}(s) = 1/s$, then it can derived that

$$\lim_{t\to\infty} e(t) = 0 \tag{5.38}$$

From (5.39), it can be found that the DC offset can be fully cancelled when the tuning loop converges.

5.9 Simulation Results

Extensive simulation of DC offset tuning at circuit level has been done with Cadence 4.4.6, HSPICE 2002.2. The result in a typical case is shown in Fig.5.21. VGA is set to the highest gain of 20 dB and DC offset is set to 10 mV. The DC offset is introduced at the time: t=10 μs. It takes 20 μs to reduce the DC offset less than 5mV. Without DC offset cancellation, the DC offset is directly amplified by the 20dB gain, and appear at the output as 100 mV DC offset.

Fig.5.22 shows the simulation results with 10% I/Q mismatch. Other simulation set up is the same as in Fig.5.21. The result shows that DC offset can be effectively suppressed under 3 mV. Furthermore, settling time is reduced to 12 μs.

The effect of varying bandwidth tuning is shown in Fig.5.23 and Fig.5.24. Fig.5.23 shows the output signal. The DC offset tuning process is shown in Fig.5.24. DC offset is introduced at the time: t=4 μs. The settling time is further reduced to 7 μs for the tuning loop to suppress the differential DC offset to less than 3mV.

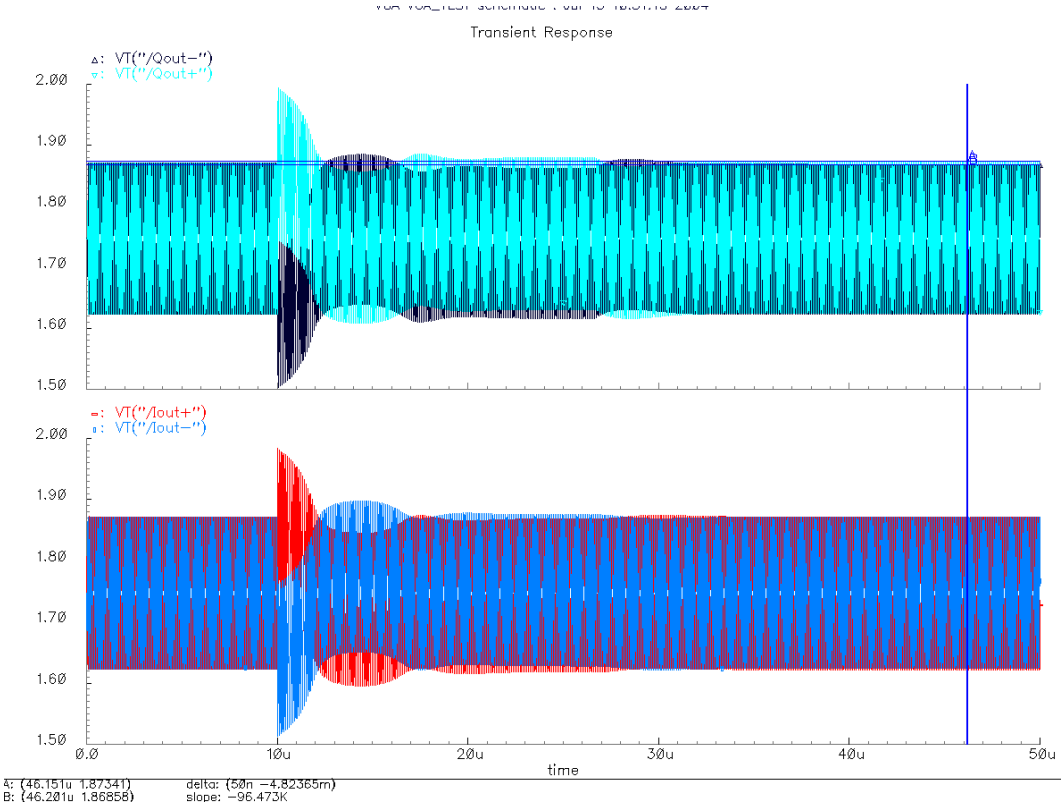


Fig.5.21 Cadence Simulation Results for DC offset tuning circuit

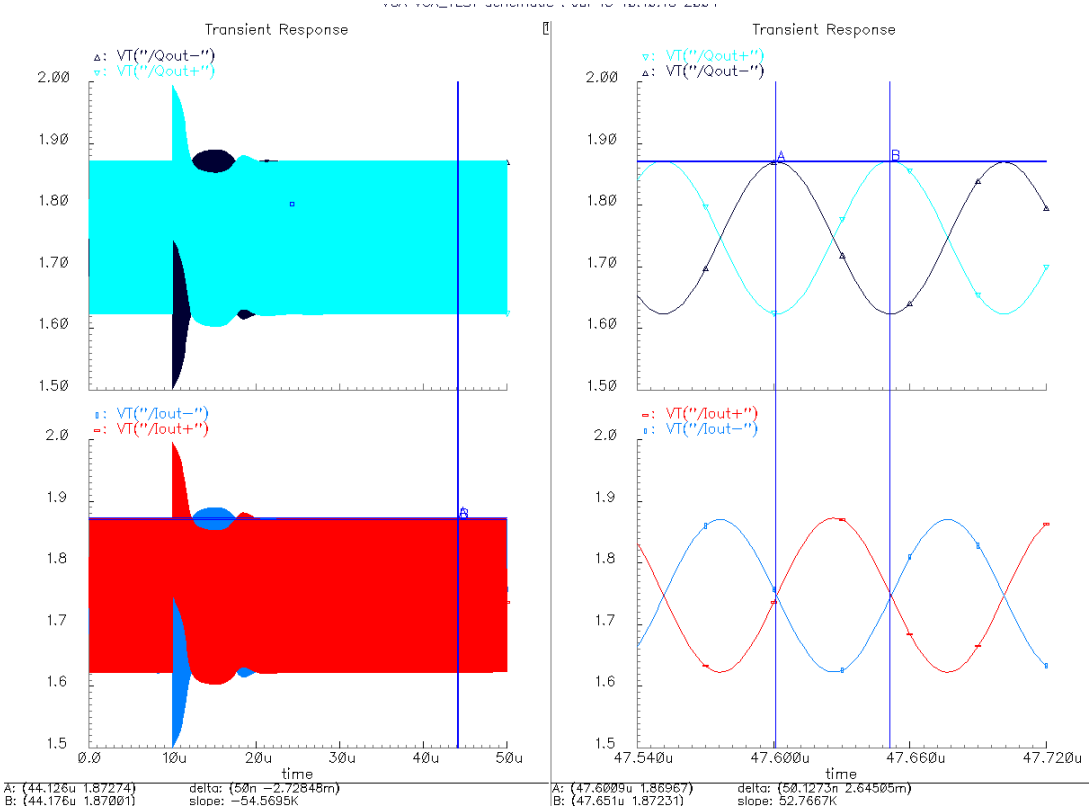


Fig.5.22 Cadence Simulation Results for DC offset tuning circuit under I/Q mismatch

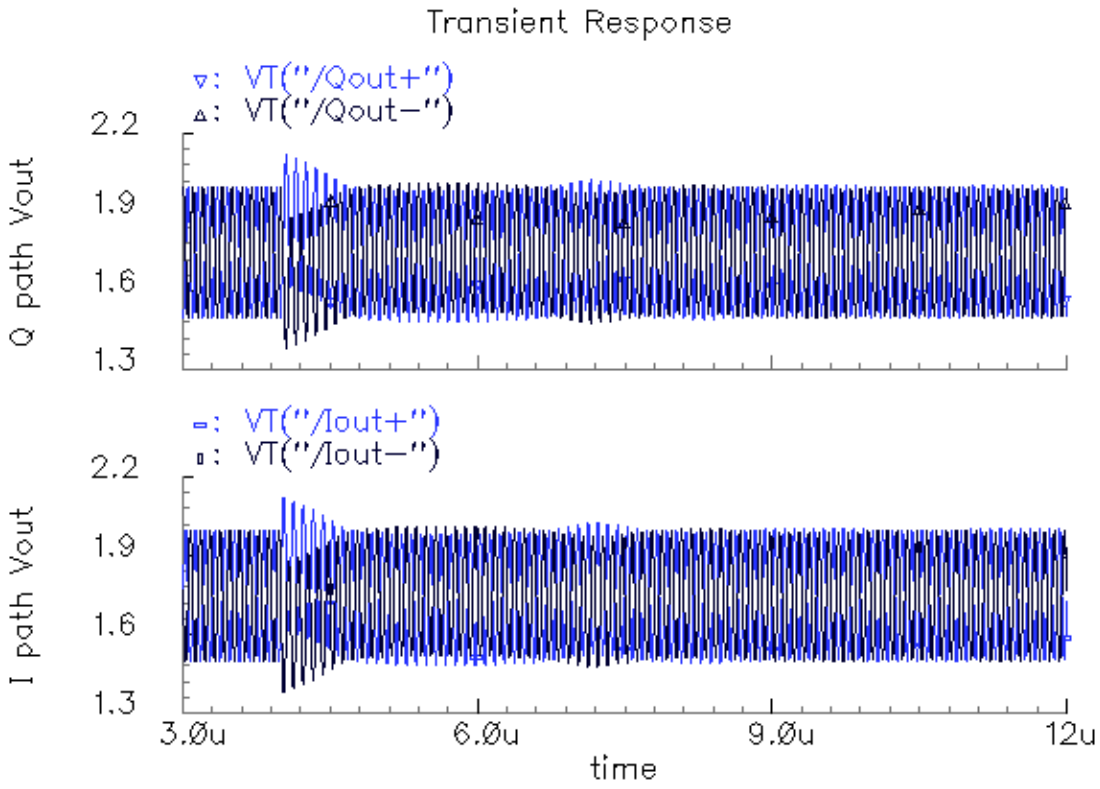


Fig.5.23 Cadence Simulation Results for Varying bandwidth DC offset tuning circuit under I/Q mismatch

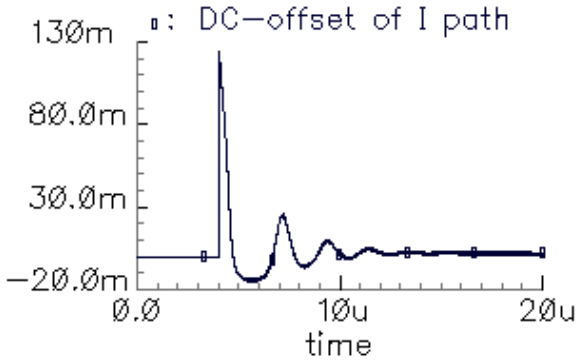


Fig.5.24 Tuning process of the DC offset with varying bandwidth under I/Q mismatch

Chapter 6

Measurement Results

The VGA chip has been fabricated using CMOS 0.35 μm technology. The layout and the die photo of the VGA chip is given in Appendix A and B respectively. The whole chip area is 1.5×1.8 mm^2, including three stages of VGA and DC offset tuning circuit, an exponential function circuit and the PTAT to provide reference current and voltage. The maximum capacitor used in this chip is 3 pf, which is small enough to be fully integrated.

The frequency response of the VGA is shown in Fig.6.1, which shows that the VGA exhibits a band-pass characteristic. Three different gain settings are used, namely, 20dB (Curve 1), 10dB (Curve 2) and 3dB (Curve 3). The high corner frequency is 2.87 MHz, determined by the VGA bandwidth, while the low corner frequency is 65 KHz, introduced by the DC offset cancellation circuit. If using AC coupling to realize such a low corner frequency, and assuming that the equivalent resistance is as large as 50 KΩ, it still need a large capacitance of 50 pf, which is too large to be implemented on chip.

The bandwidth of the VGA is larger than specification (2.5 MHz) and the low corner frequency is very low so that its effect on the desired signal is little. The gain of the VGA can be varied continuously from -1 dB to +20.13 dB.

Due to the limitation of the test instrument, the frequency response at DC can not be displayed directly. Based on the slope of -10dB/dec for the low frequency roll-off, we could extrapolate the curve for 5 decades from the 3 dB bandwidth 65 KHz to 6.5 Hz. Therefore, the VGA has a DC rejection of 50 dB.

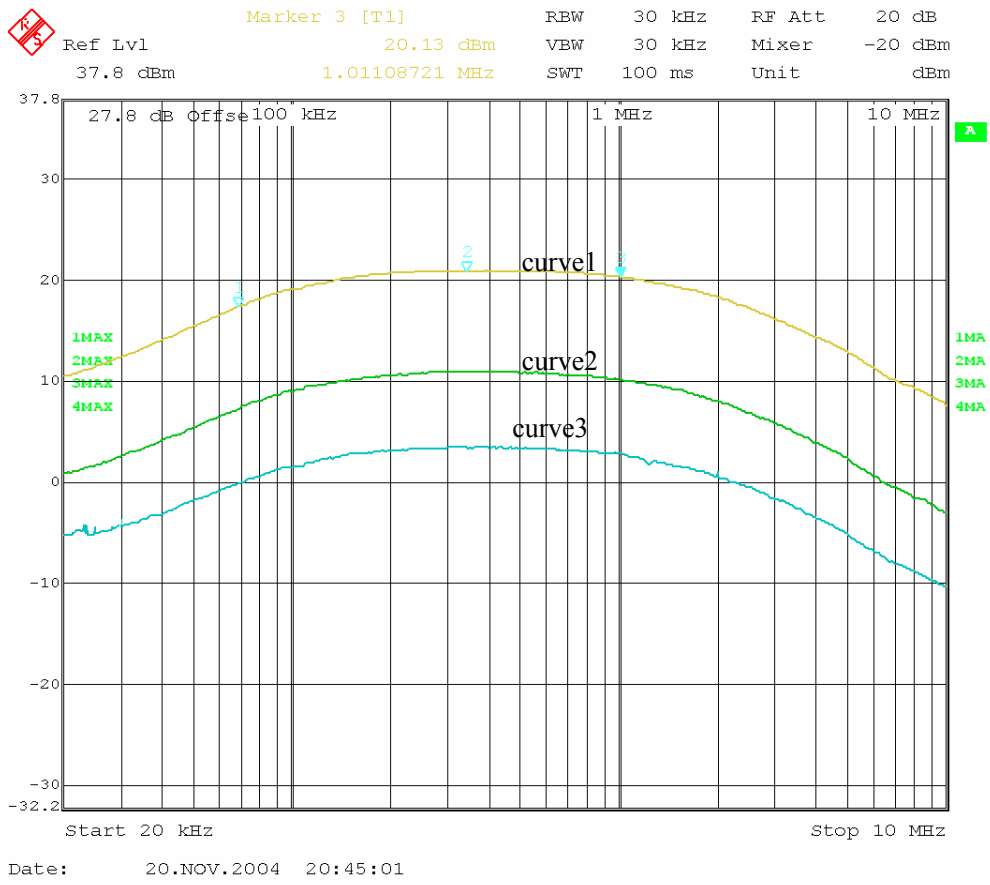


Fig.6.1 Frequency Response of the VGA

Fig.6.2 shows the measured receiver two-tone test output spectrum. The two tone input signals are at 1.4 and 1.6 MHz with power levels of -12.48 dBm. The third-order intermodulation product, which is located at 1.8 MHz, is 49.29 dB below the main signal. This translates to an input-referred third-order intercept point (IP3) of 12.165 dBm. Similarly, the second-order intermodulation product, which is located at 3.0 MHz, is 53.19 dB below the main signal. Therefore, the input-referred second order intercept point (IP2) of the VGA is 40.7 dBm.

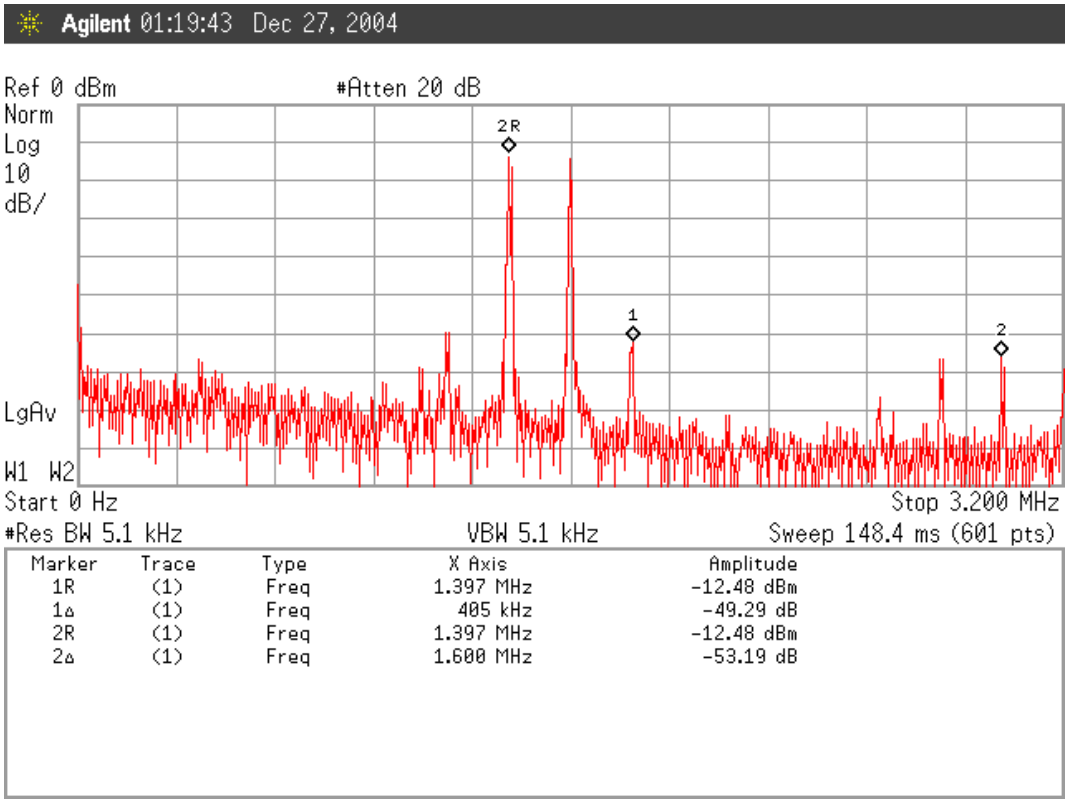


Fig.6.2 Two tone test of the VGA

Measurement result of the pseudo-exponential voltage circuit is shown in Fig.6.3. Good approximation to exponential voltage can be achieved when input

voltage V_{in} in the range of (0, 0.8V) and (1.5 V, 2.5 V). In the range of $0.8\text{V} < V_{in} < 1.5\text{V}$, the curve exhibits a faster increasing rate, this is due to the compensation techniques described in Chapter 4. A current $I_{CS} > 4I_o$ is used in the CSC to make the rate of the gain variation versus the control voltage V_{ctrl} when V_{in}^c is high faster than that defined by the exponential function. This pre-distortion technique is used to compensate the nonlinear effect in dB-linear. However, when the input voltage of the exponential circuit goes very large, that is, the output current of the V-I convertor, I_{VI} is very large, a larger current $I_{VI} + I_{CS}$ goes into the CSC and may make the transistors not in saturation. Therefore, in this range, the CSC can not provide a perfect square current, making the output voltage can not increase faster than an ideal exponential function.

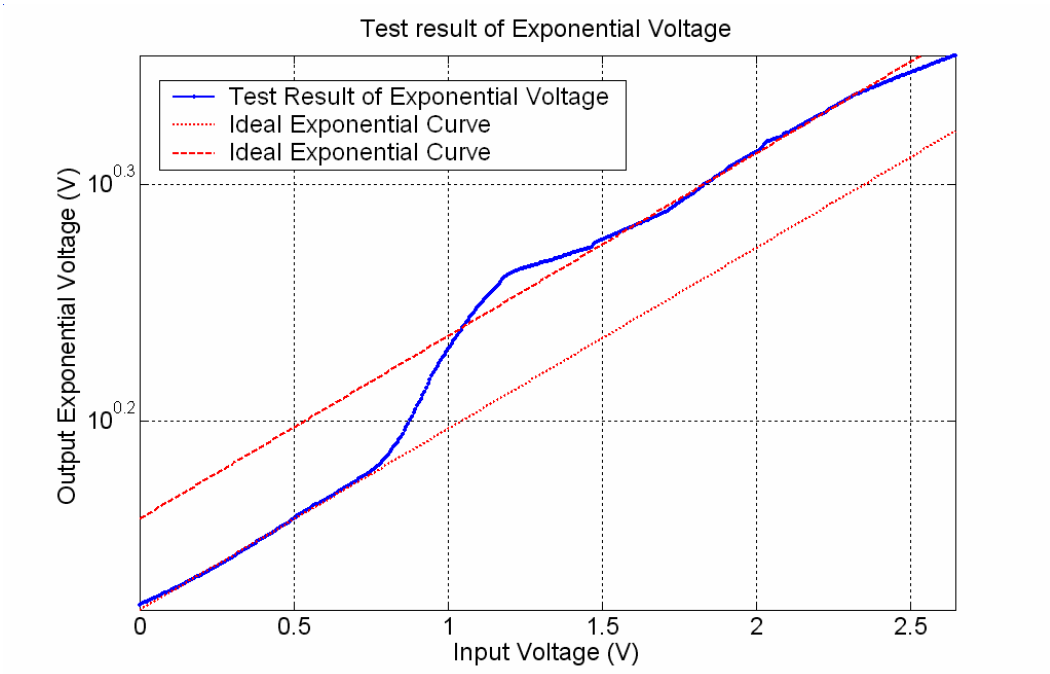


Fig.6.3 Test result of Exponential Voltage

Measurement result of dB-linearity of the proposed VGA is shown in Fig.6.4. It can be shown that when V_{ctrl} >1.2 V, the linearity curve begins saturation. This is caused by the non-linearity effect analyzed in Chapter 4. And since after Vctrl>1.2 the pseudo-exponential voltage does not go faster than an ideal exponential voltage, it can not provide compensation to the non-linearity effect. The gain range is 0-20dB when V_{ctrl} in the range of (0, 2.7V), as compared to 20 dB obtained in simulation for V_{ctrl} from 0 to 1.2V. This may be because when the compensation current is added to the CSC in Fig.4.3, the input current is too large and causes the CSC circuit to saturate.

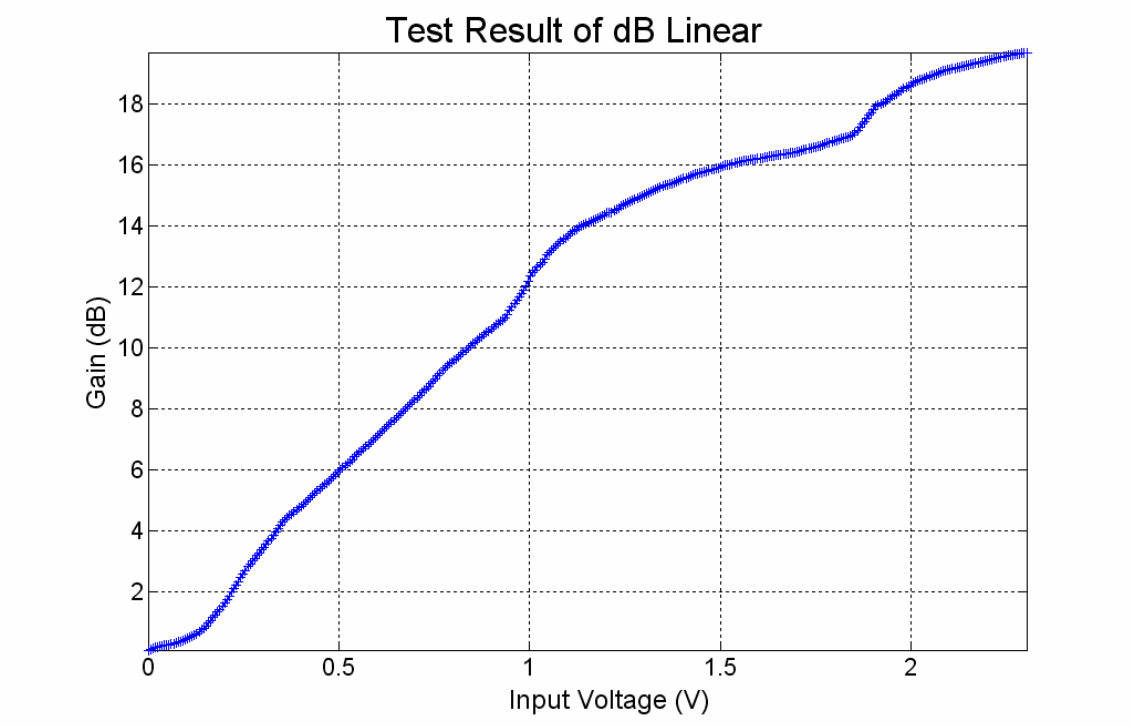


Fig.6.4 Test result of dB linear

Measurement results of the DC offset cancellation are shown in Fig.6.5. A DC offset is intentionally added at the input of VGA, and the output DC voltage is

measured at the output. VGA is set to the highest gain of 20 dB. The final output DC offset versus the input DC offset is shown. The output DC offset can be suppressed effectively when input DC offset is less than 120 mV. The highest output DC offset is 14 mV. However when input DC offset is higher than 120 mV, the DC offset cancellation circuit can not work effectively. Because in practice applications, the DC offset coming from the mixer will not exceed 100mV, the DC cancellation ability of the tuning loop has met the requirement of DCR.

The measurement results are collected in Table III.

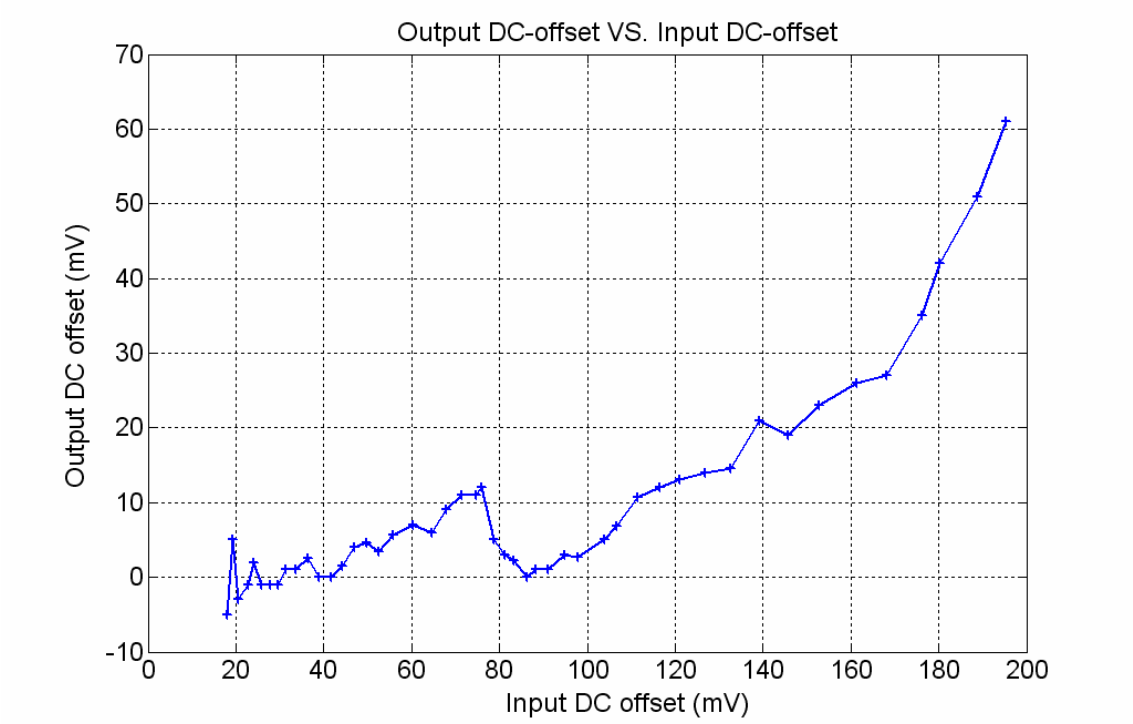


Fig.6.5 Output DC offset of the VGA

Table 3 Measurement results

Gain range	0-60 dB
Bandwidth	2.87 MHz
IIP3	12.165dBm
IIP2	40.7dBm
Output DC offset	<14mV

Chapter 7

Conclusion and Recommendation

Conclusion

A dB-linear VGA with DC offset cancellation for Direct Conversion Receiver has been proposed and implemented in a 0.35-μm CMOS technology. The VGA has achieved a gain control range over 60-dB. With a newly proposed exponential function generation circuit, good dB linearity can be obtained for the input voltage range up to 1V. The DC offset cancellation is realized with a new I/Q tuning technique. The proposed I/Q tuning loop can suppress the DC offset and the I/Q mismatch due to DC offset simultaneously. The measured results show that output DC offset is less than 14 mV when input DC offset is less than 120 mV. With the varying bandwidth circuit, the tuning (or the DC cancellation) is able to settle within 7 μs according to the simulation. Some problems are also encountered in the first prototype chip, such as dB linearity at high input, which will be further analyzed and considered in the future work.

Recommendations

1) It has been observed that the dB-linearity is degraded at high input voltage. Possible causes have been analyzed in Chapter 6. Further investigation needs to be carried out to pin down the problem and improve it in the future design.

2) In consistent DC offset rejection has been observed during the measurement. Possible causes need to be further investigated in the future work.

3) The suppression of I/Q mismatch may be further improved in the future work with simple or more effective technique and circuit.

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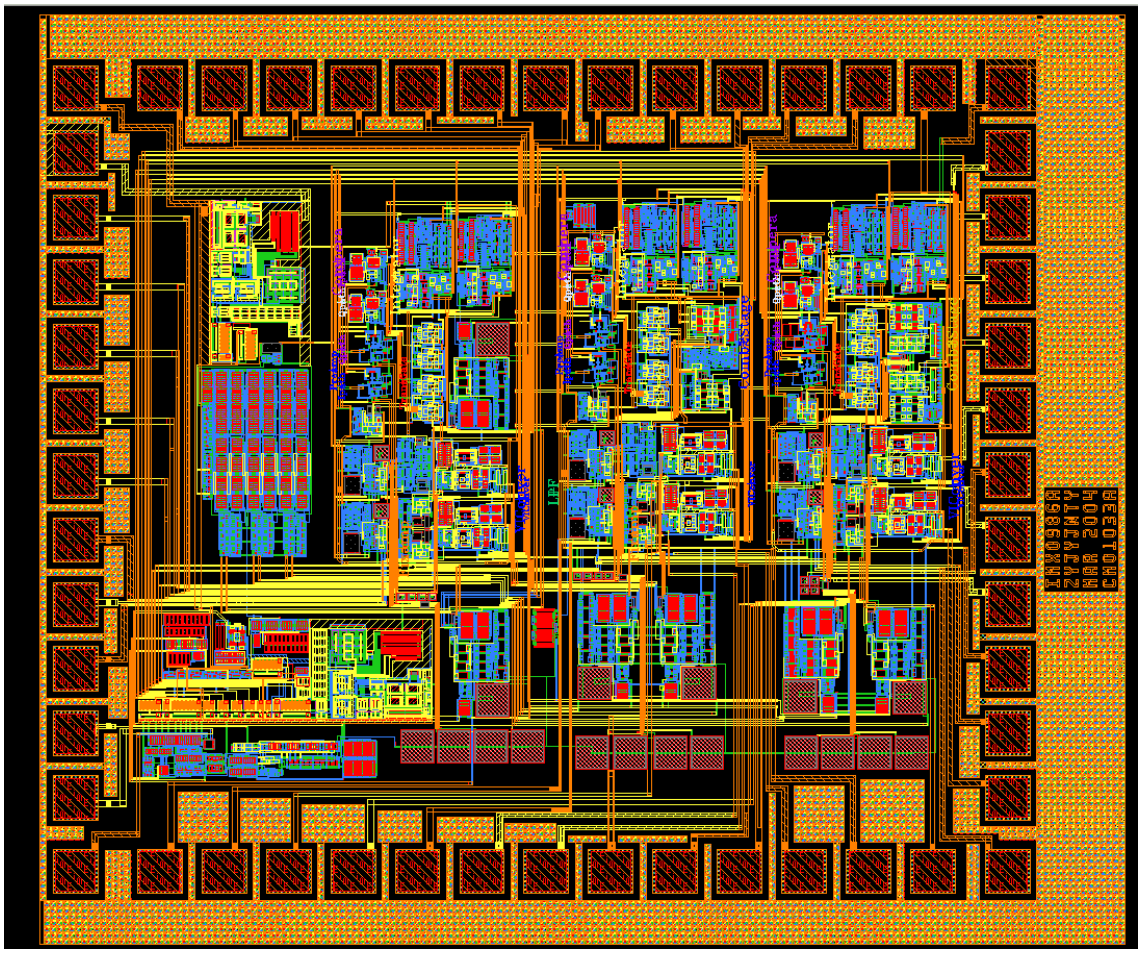
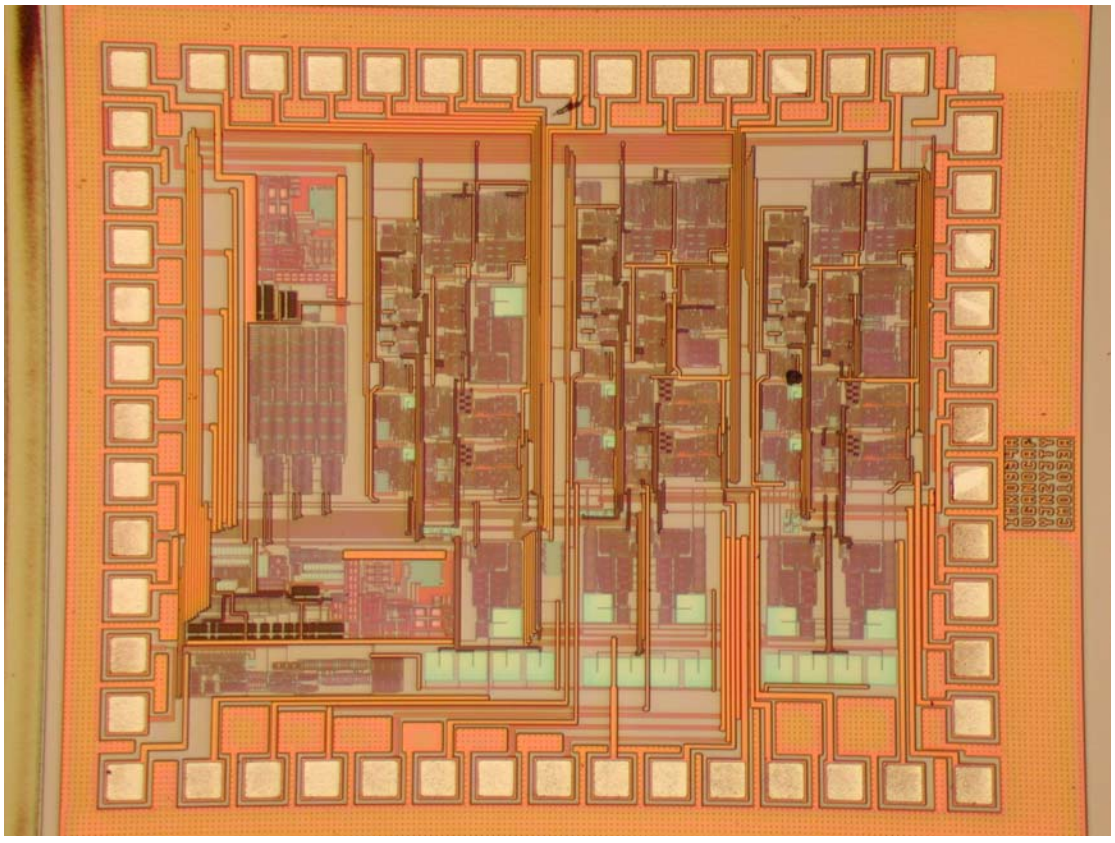
Appendix A

Layout of the VGA chip



Appendix B

Die Photo



Appendix C

Publications

P1: Yuanjin Zheng, Jiangnan Yan, Yong Ping Xu, *"***A CMOS dB-linear VGA with pre-distortion compensation for wireless communication applications**"**,** *IEEE International Symposium on Circuits and Systems*, vol. 1, pp.I-813-16, 2004.

P2: Jiangnan Yan, Yuanjin Zheng, Yong Ping Xu, "**A novel DC offset Canceling Circuit for DCR**", *IEEE International Symposium on Circuits and Systems,* pp. 396-399, May 2005.